

**COMPAL  
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MODEL NAME : **CAP00**

PCB NO : **LA-E311P**

BOM P/N : **431A4X31L01**

GPIO MAP: **Gen7 GPIO Master\_XXXX**

# CRANE15

**Kaby Lake H-type (2 chip)**

**REV : 1.0(A00)**

**2016.11.21**

**@ : Nopop Component**

**EMC@ : EMI/ESD/RF part**

**CONN@ : Connector Component**

**XDP@ : Total debug Component (pop them until ST)**

Layout Dell logo



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REV: X00  
PWB: XXXXX  
DATE: 1403-06

PCB ITS LA-E311P REV0 MB 1

Part Number	Description
DAA000CS010	PCB ITS LA-E311P REV1 MB 1

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**Cover Sheet**

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## POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE			RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

## PM TABLE

State	power plane	+PWR_SRC +5V_ALW +3.3V_ALW +3.3V_ALW2 +3.3V_ALW_DSW +3.3V_ALW_PCH +3.3V_RTC_LDO +1.8V_ALW +1.0V_PRIM	+3.3V_SUS +1.2V_MEM +2.5V_MEM +1.0V_VCCST	+5V_RUN +3.3V_RUN +1.5V_RUN +0.675V_DDR_VTT +3.3V_MXM +5V_MXM +MXM_PWR_SRC	(M-OFF) +VCC_CORE +VCC_EDRAM +VCC_EOPIO +VCC_GTU +VCC_GT +1.0V_VCCSTG +VCC_SA
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

SATA	DESTINATION
SATA 0	2280 SSD
SATA 1	Dock ESATA
SATA 2	NA
SATA 3	SATAe HDD
SATA 4	M.2 Slot-2 (cache)
SATA 5	NA

## Stack up

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil
			SolderMask	IT-158
1	Top	3.7	Copper foil	0.5oz
2	GND/PWR	3.7	Prepreg	1050
3	Sig 1	4.1	Copper foil	1oz
4	GND/PWR	3.7	Prepreg	2116Mx2
5	Sig 2	3.7	Copper foil	1oz
6	Sig 3	3.8	Prepreg	1050Hx2
7	GND/PWR	3.7	Copper foil	1oz
8	Sig 4	4.1	Prepreg	2116Mx2
9	GND/PWR	3.7	Copper foil	1oz
10	Bottom	3.7	Prepreg	1050
			SolderMask	0.5oz
Overall Thickness (1.45mm ± 10%)				57.09

USB3.0	DESTINATION
Port 1	Left Side JUSB1
Port 2	M.2 Slot-2 (WWAN/LTE/HCA)
Port 3	Right Side JUSB1
Port 4	Right Side JUSB2
Port 5	Right Side JUSB3
Port 6	Docking

USB PORT#	DESTINATION
1	Left Side JUSB1
2	Right Side JUSB1
3	Right Side JUSB2
4	Right Side JUSB3
5	Docking USB3.0
6	M.2 Slot-1 (BT)
7	Docking USB 2.0
8	M.2 Slot-2 (WWAN/LTE/HCA)
9	Touch Screen
10	USH
11	Camera
12	NA
13	NA
14	NA

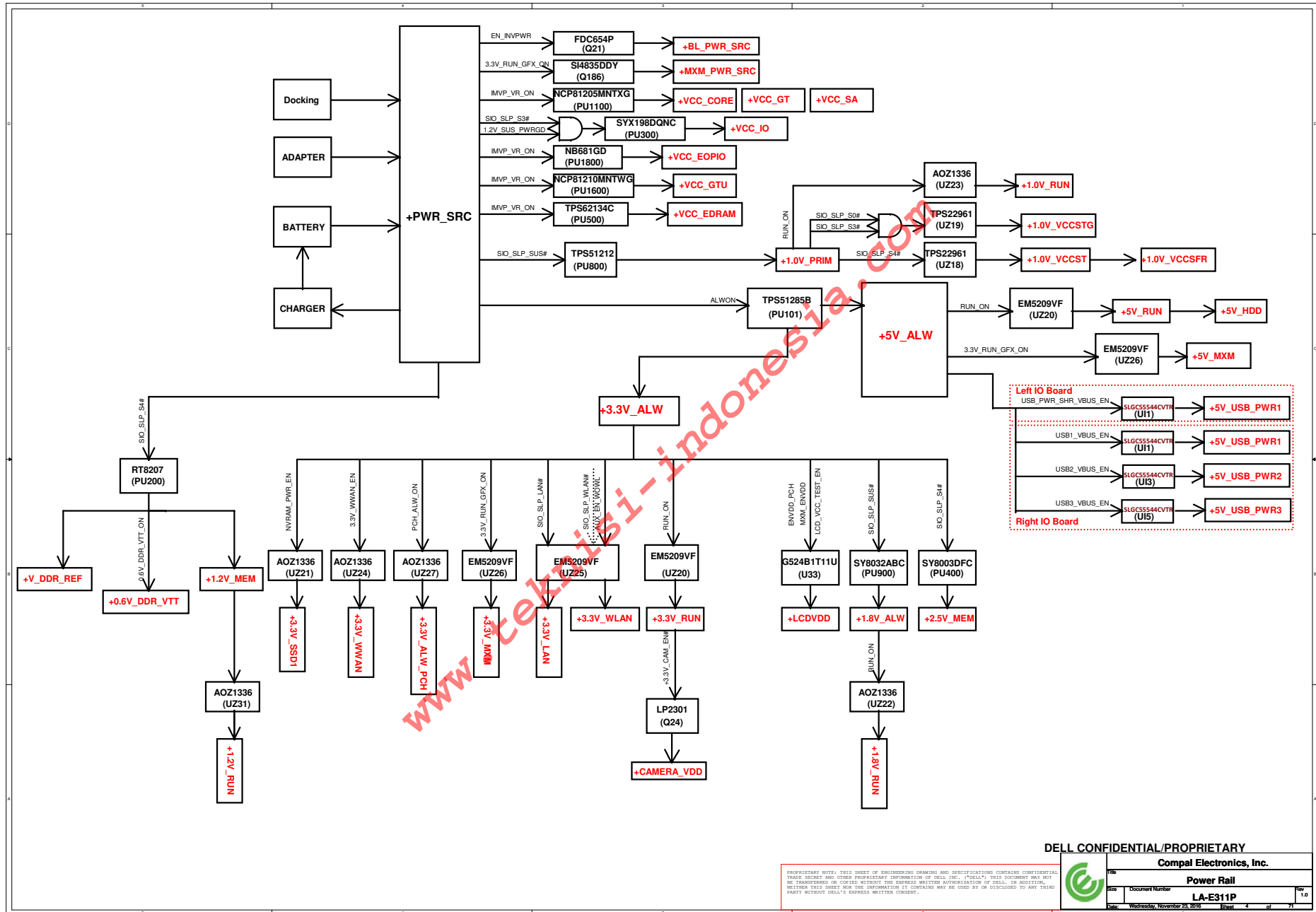
USH		BIO
0		NA
1		NA

PCI EXPRESS	DESTINATION
Lane 1	NA
Lane 2	M.2 Slot-1 (WLAN)
Lane 3	MMI(Card reader)
Lane 4	10/100/1G LOM
Lane 5~8	TBT-Alpine Ridge
Lane 9~12	M.2 Slot-3(SSD 2280)
Lane 13~14	(Dock ESATA),NA(LANE reservsal)
Lane 15~16	SATA-Express HDD(LANE reservsal)
Lane 17~18	M.2 Slot-2(WWAN/LTE/Optane)

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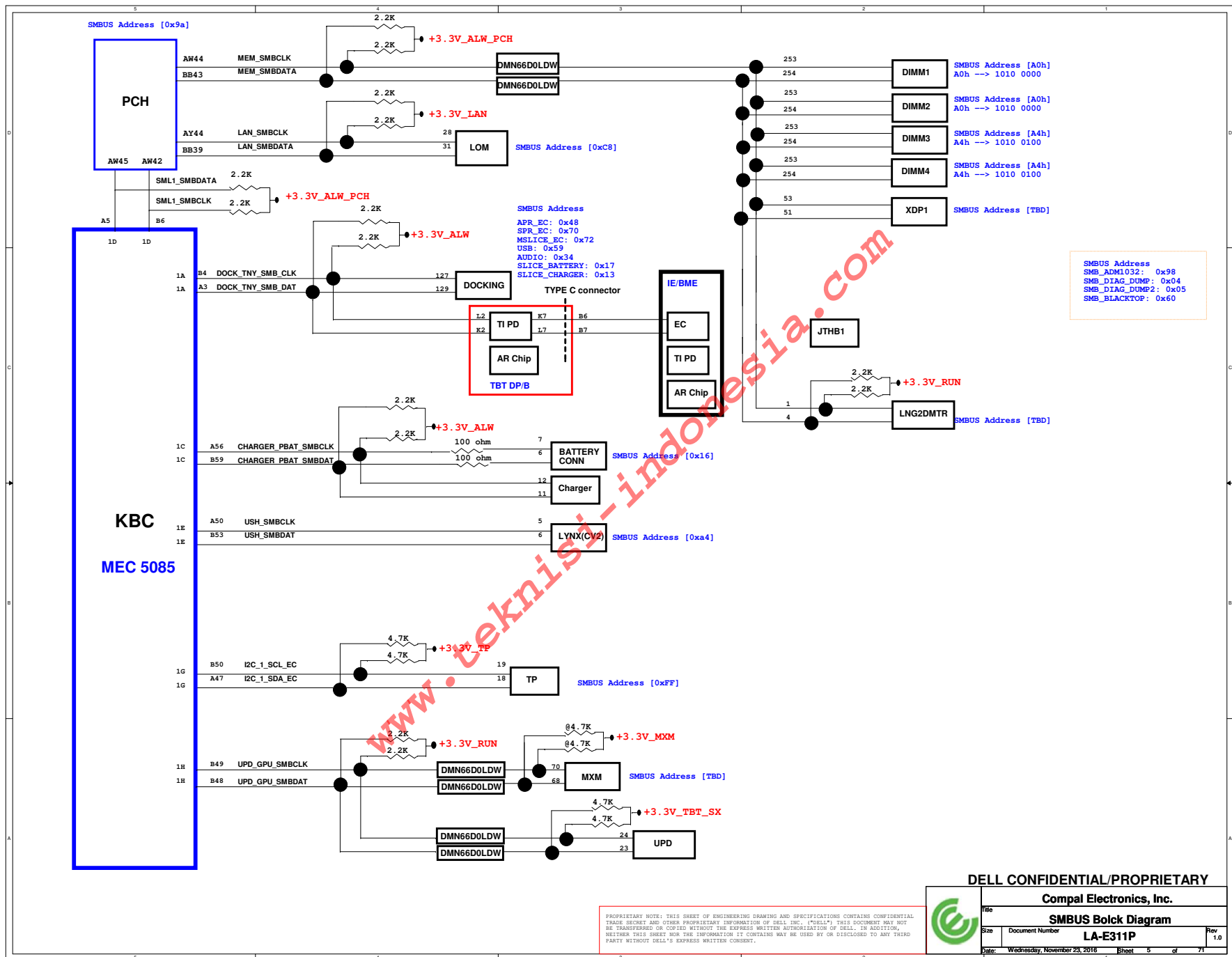
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LA-E311P

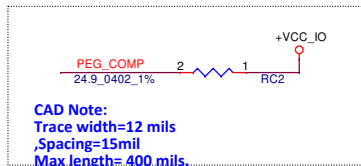
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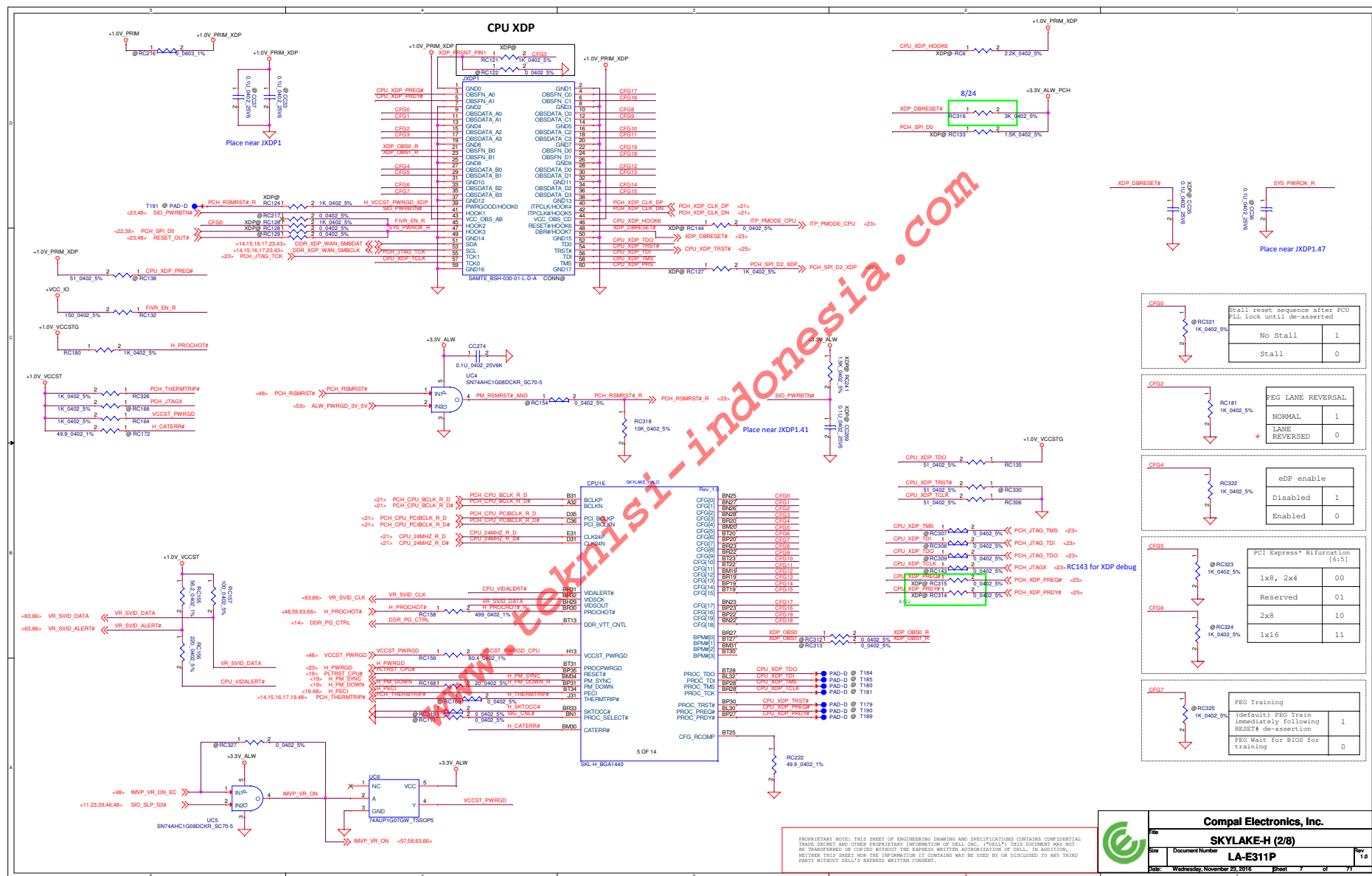
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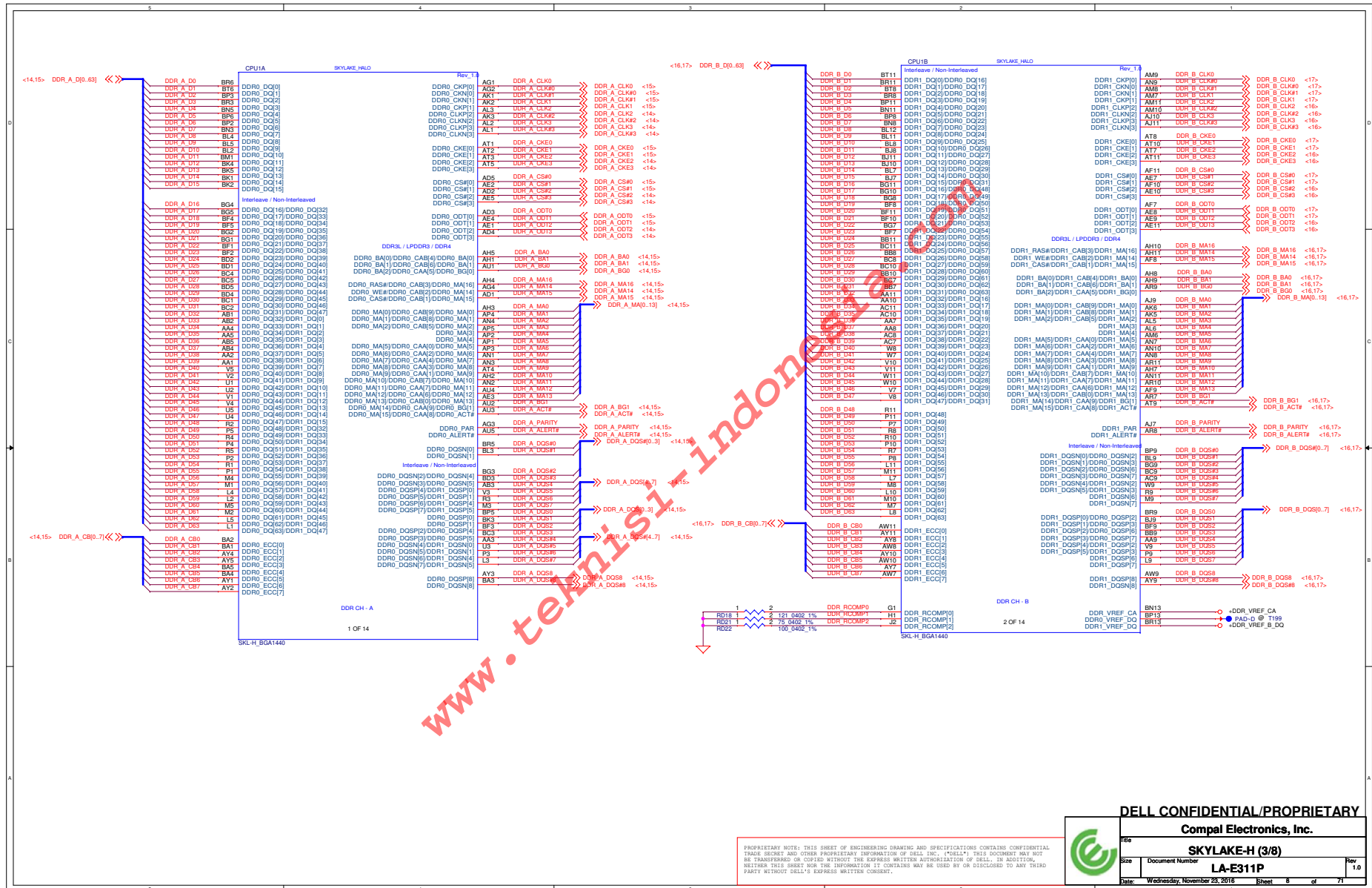
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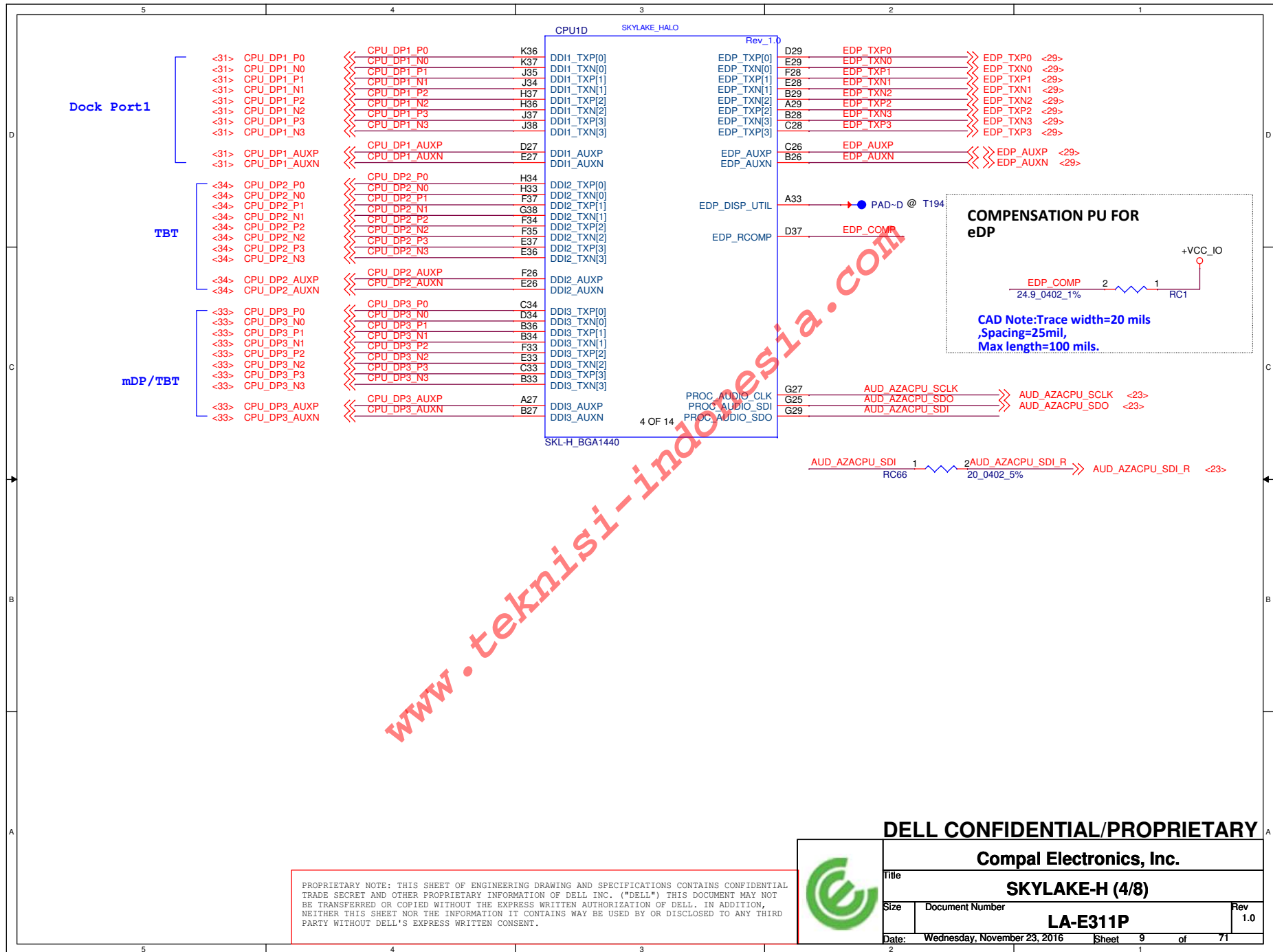
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Title SKYLAKE-H (1/8)			
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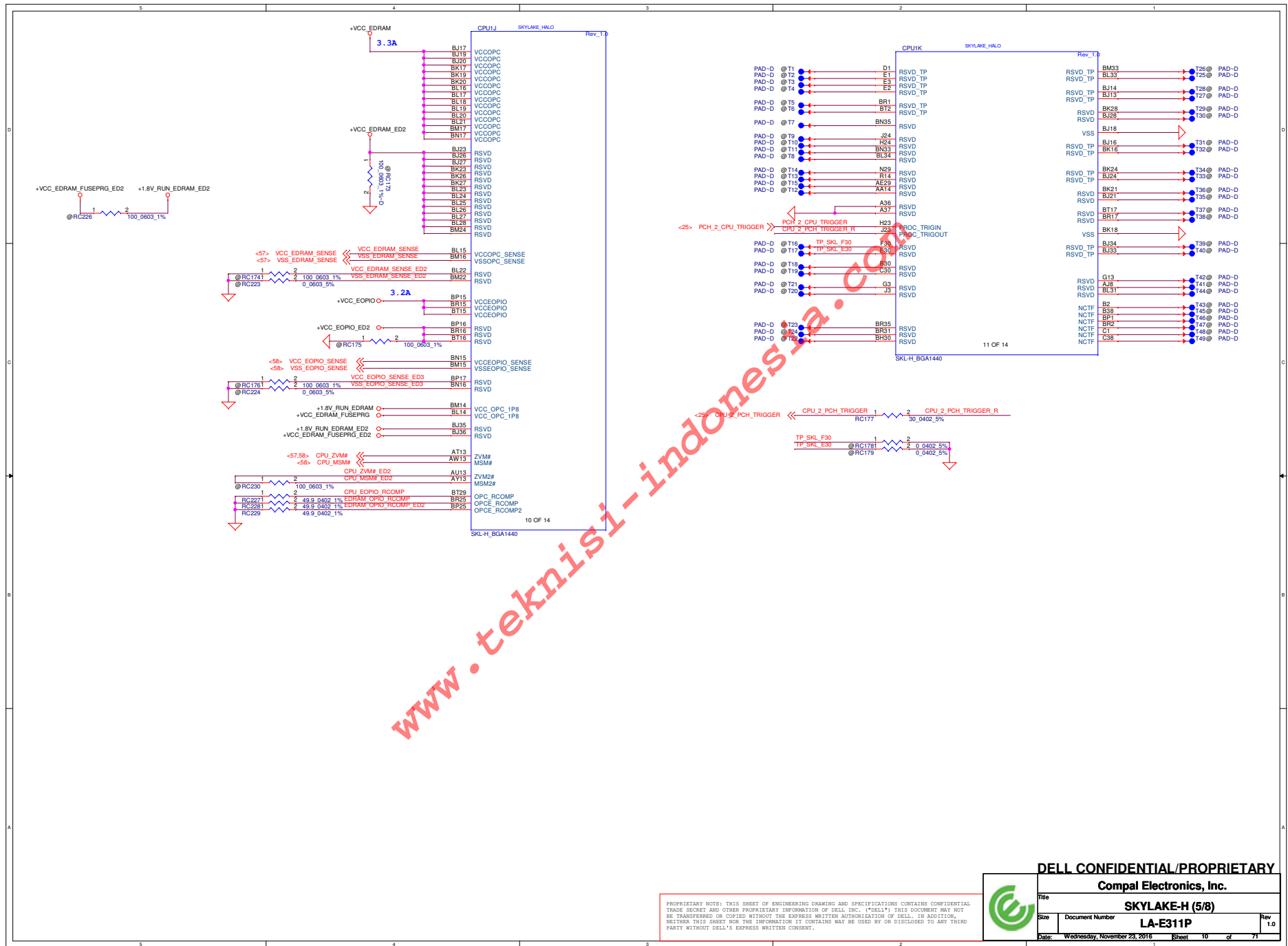
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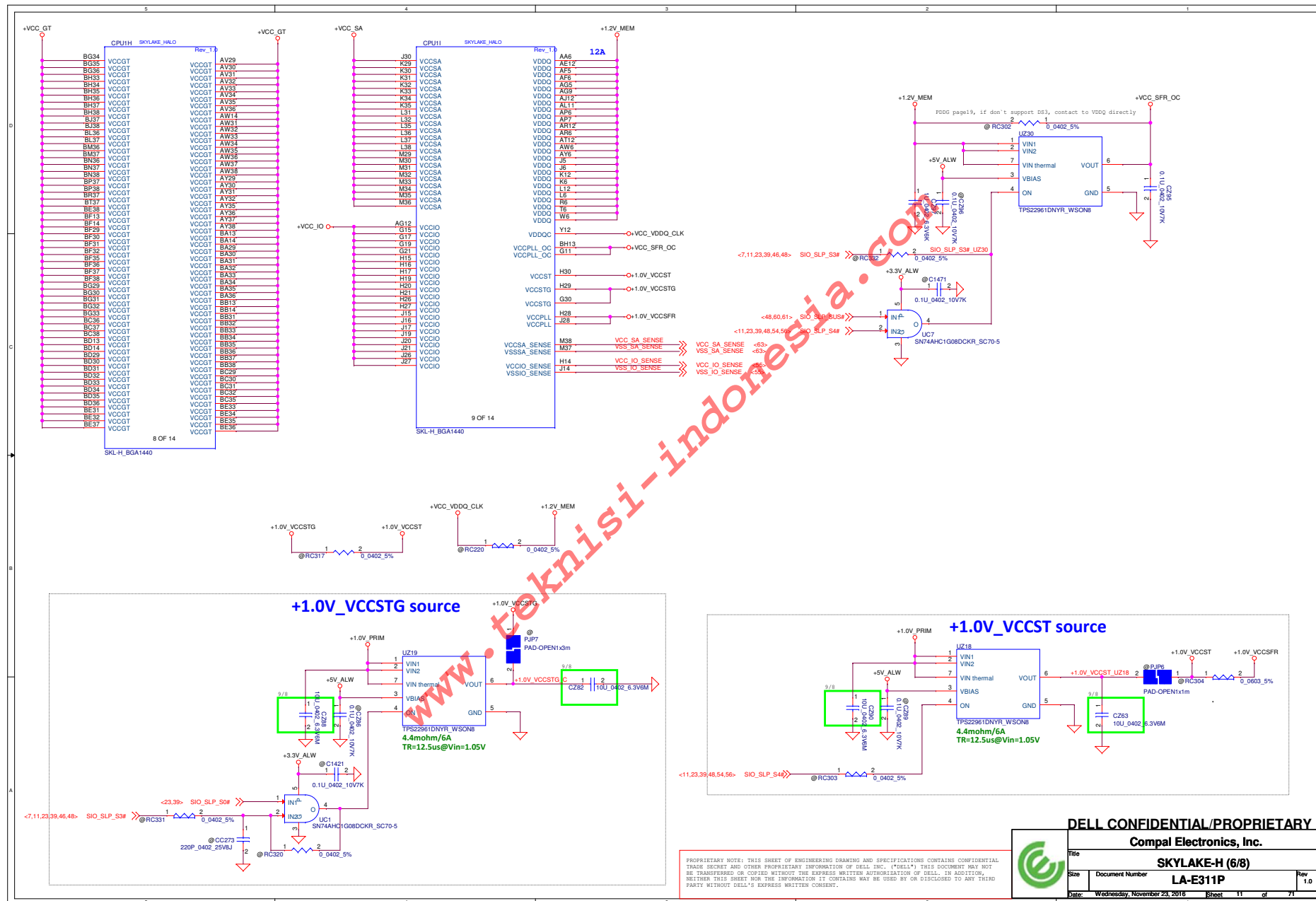


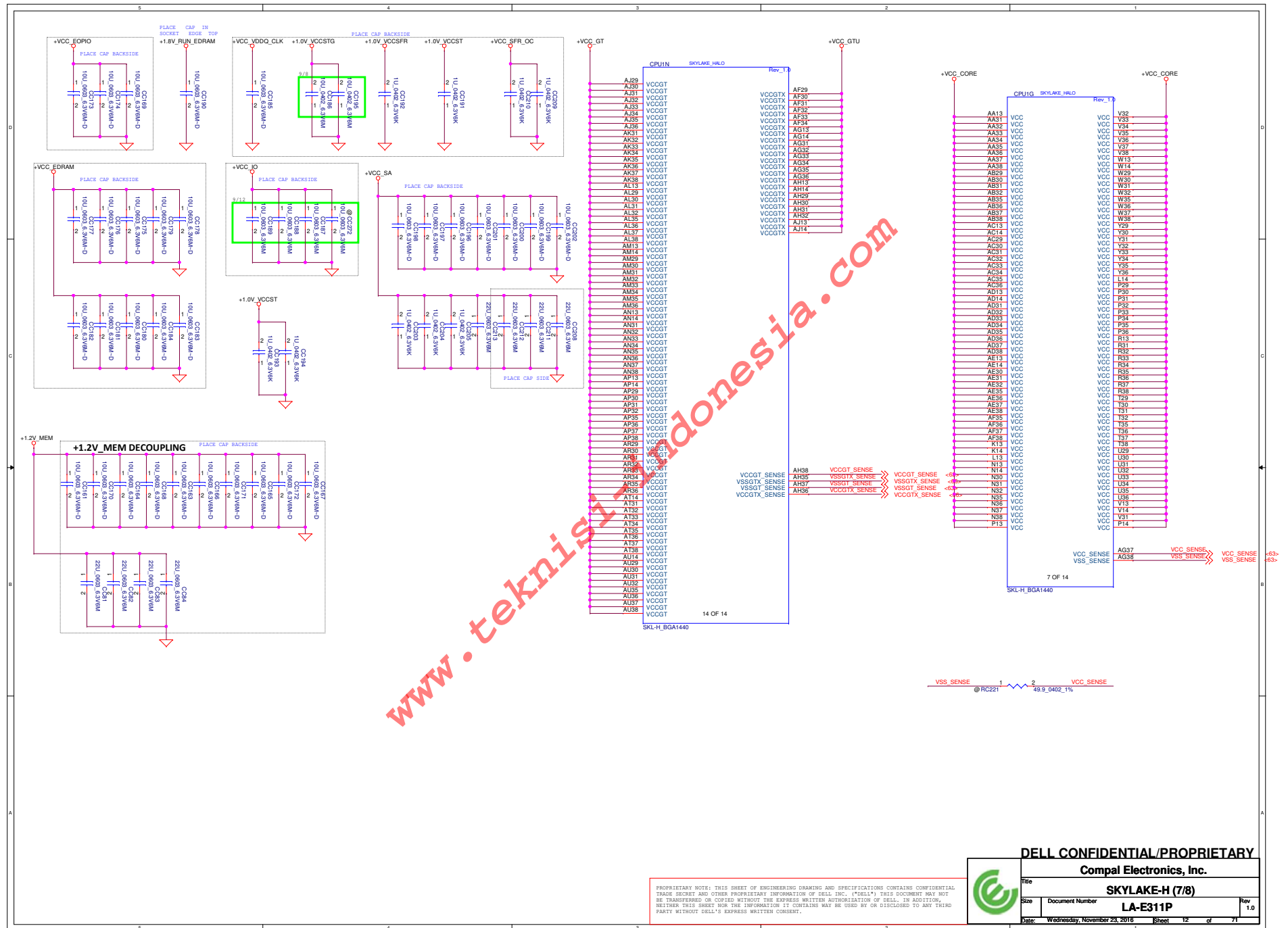
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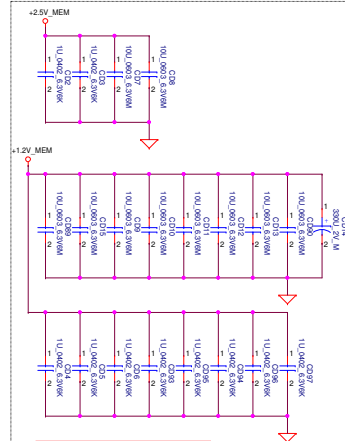




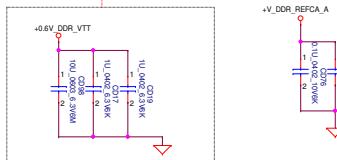


All VREF traces should have 10 mil trace width

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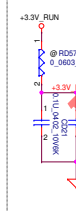
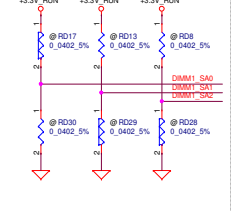


Layout Note:  
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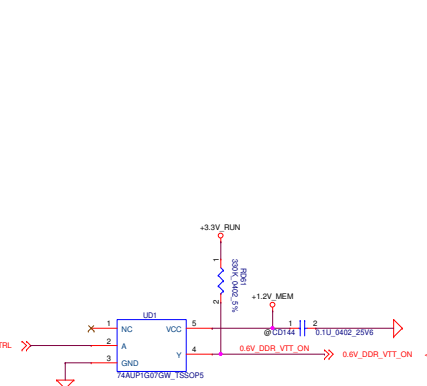
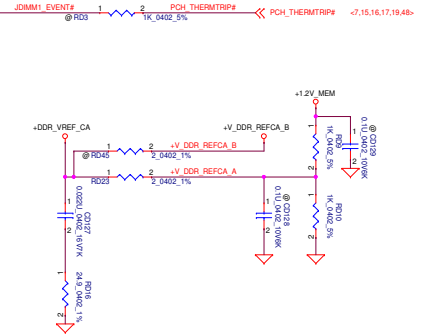
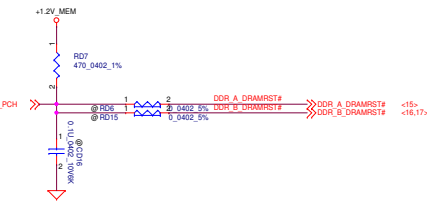
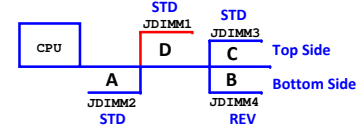


### DIMM Select

	SA0	SA1	SA2
DIMM2	0	0	0
DIMM4	0	1	0
DIMM1	1	0	0
DIMM3	1	1	0



<7.15,16,17,23,43> DDR\_WD\_PAN\_SMBCLK <<>



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DDRIII-SODIMM SLOT1

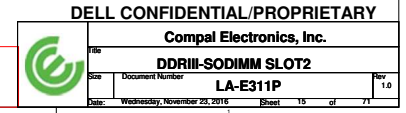
LA-E311P

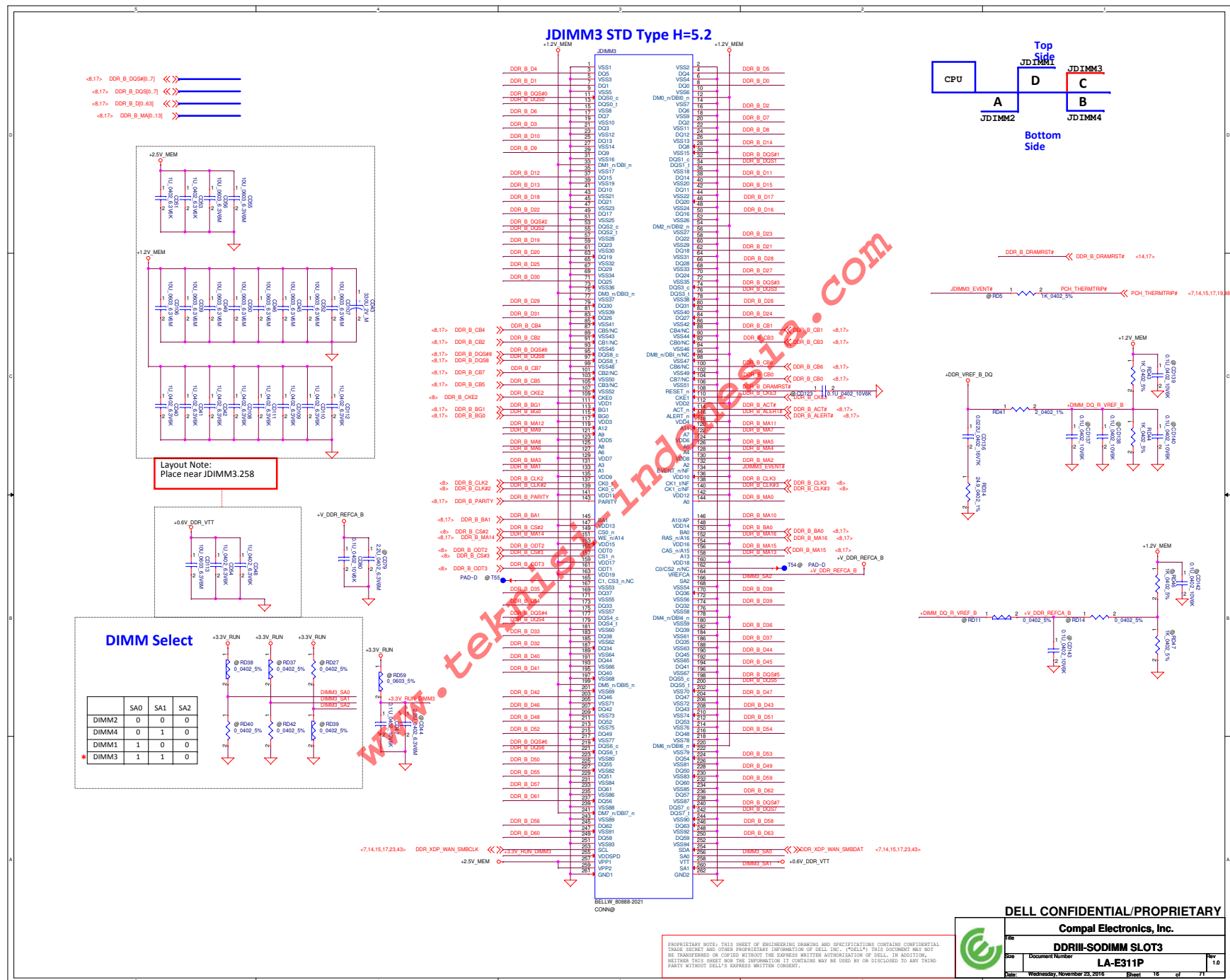
Document Number

Wednesday, November 25, 2016

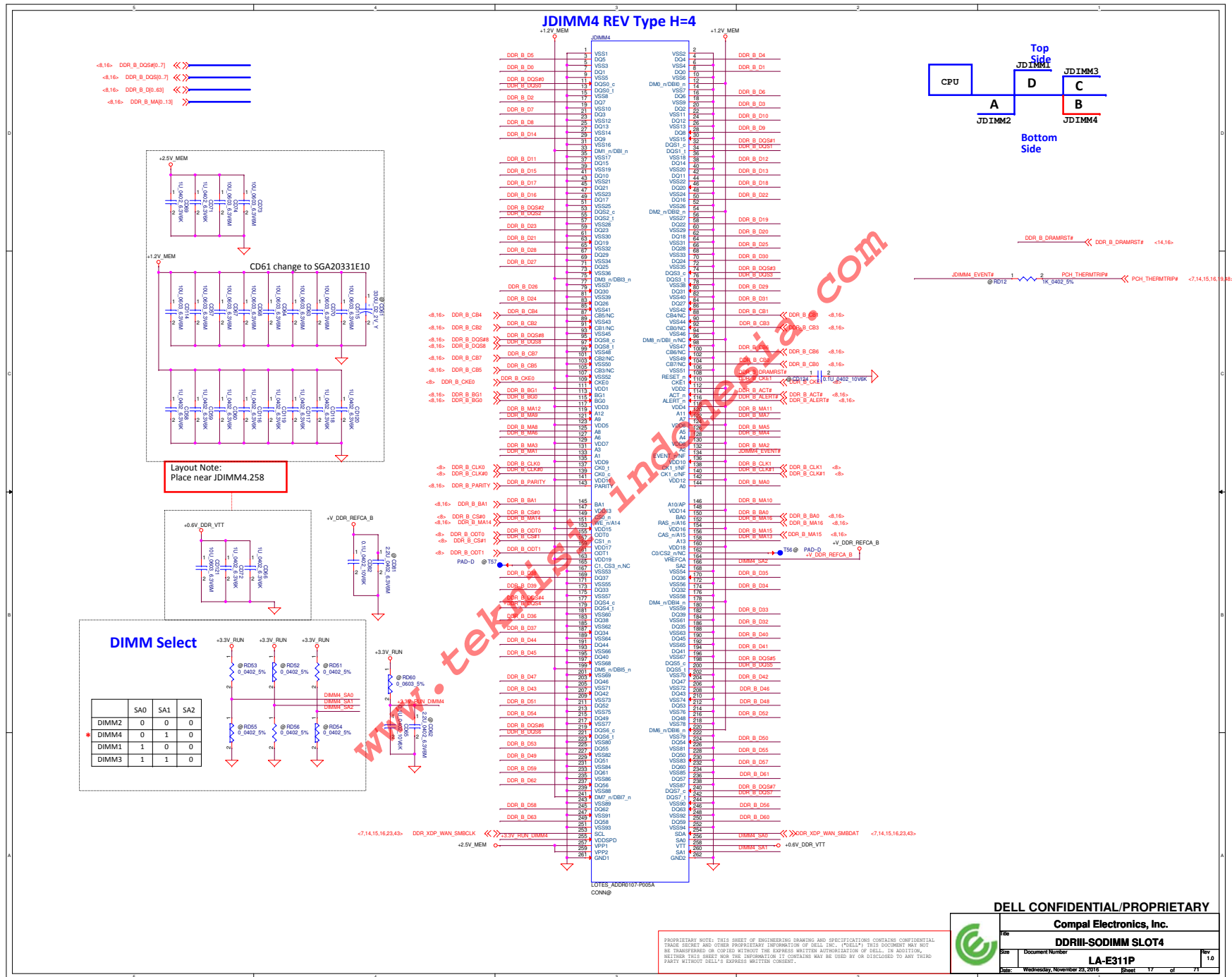
Sheet 14 of 71

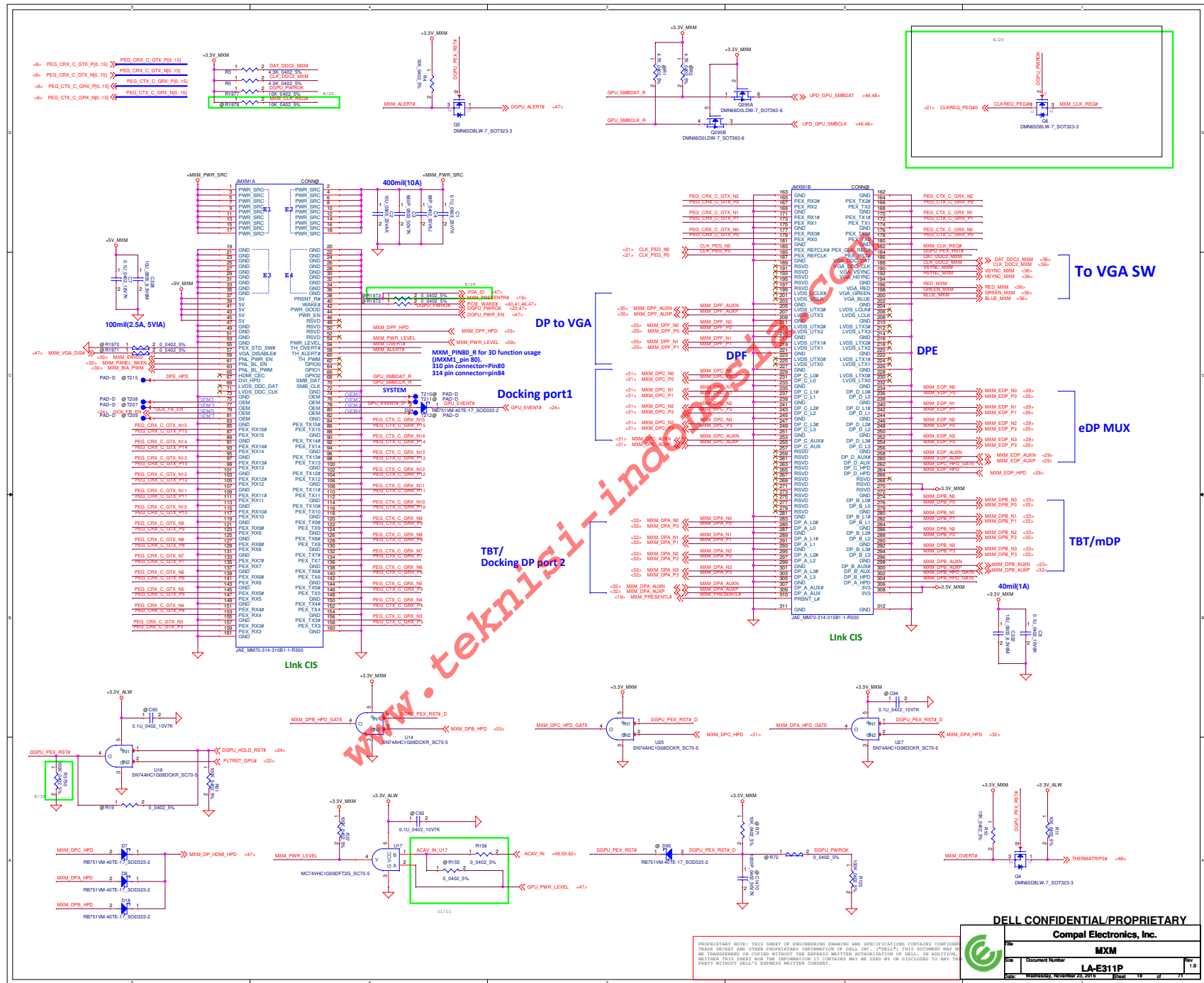
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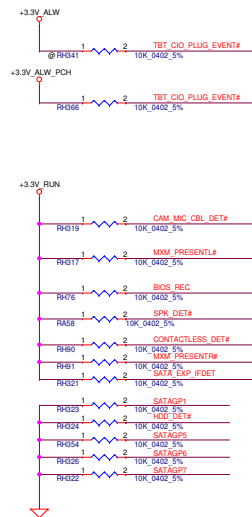










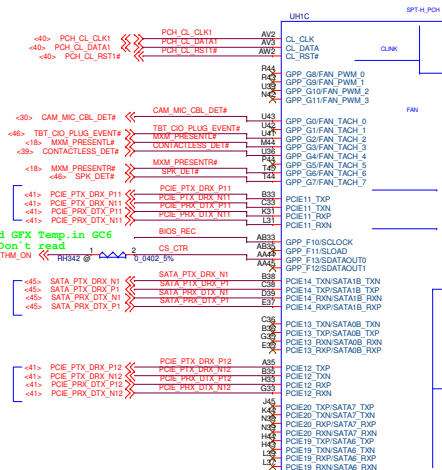


Tell EC don't read GFX Temp.in GC6  
High: Read; Low: Don't read

M.2 SSD Slot#3

Dock

M.2 SSD Slot#3

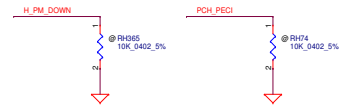


M.2 SSD Slot#3

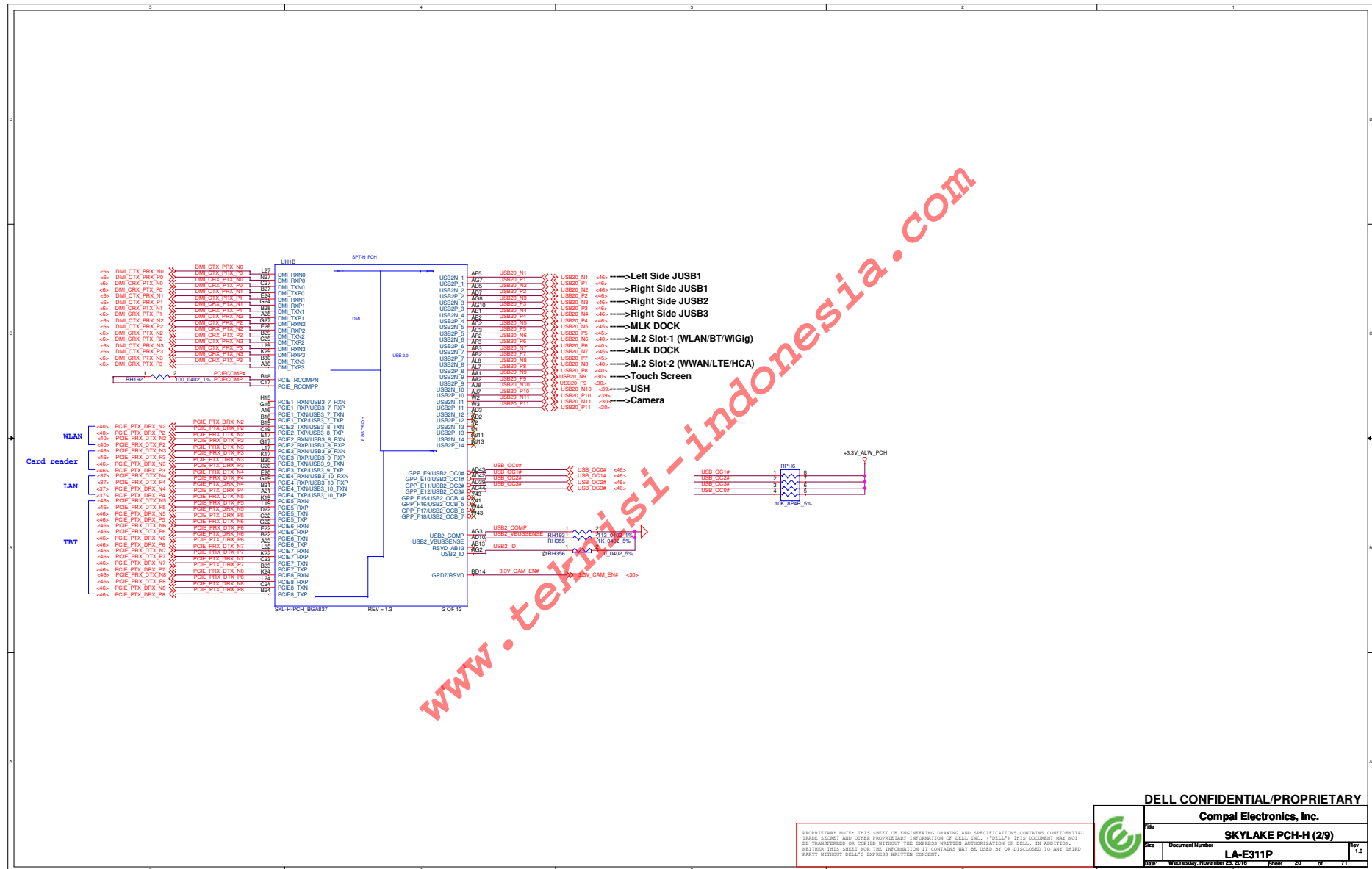
SATA Express

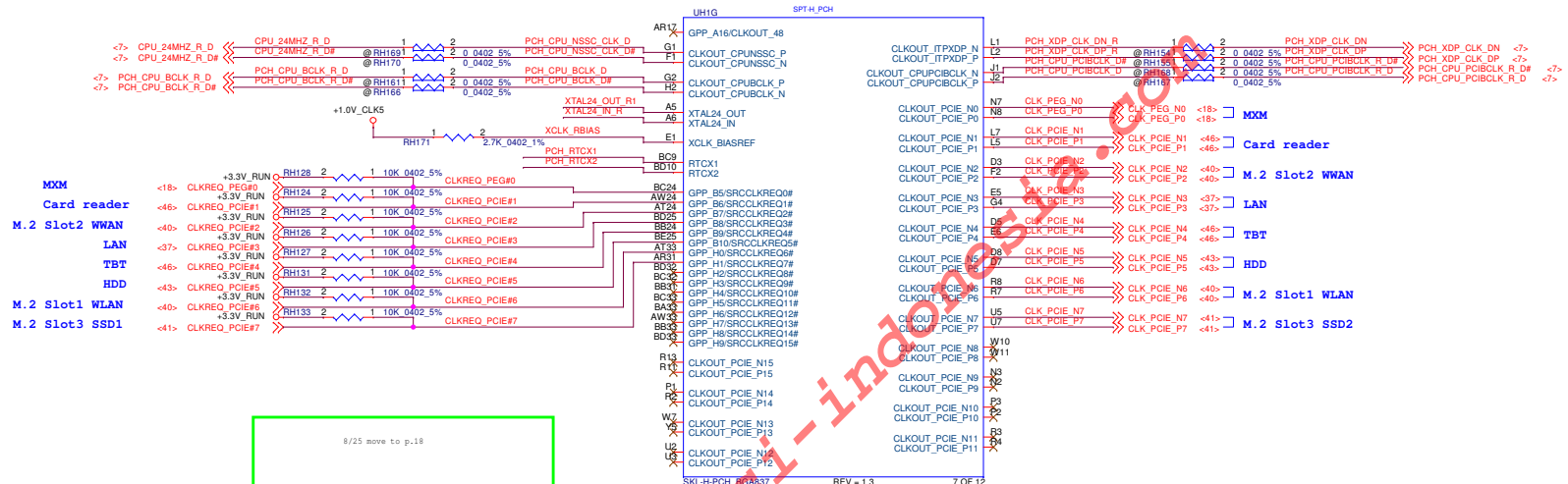
M.2 SSD Slot#4

SPSGP0	1	M2_SLOT3_PDET	0=SATA	1=PCIE
SPSGP3	0	SATA_EXP_IFDET	0=SATA	1=PCIE
SPSGP4	1	M2_SLOT2_PCIE#_SATA (SLOT2_CONFIG_1)	0=SATA	1=PCIE



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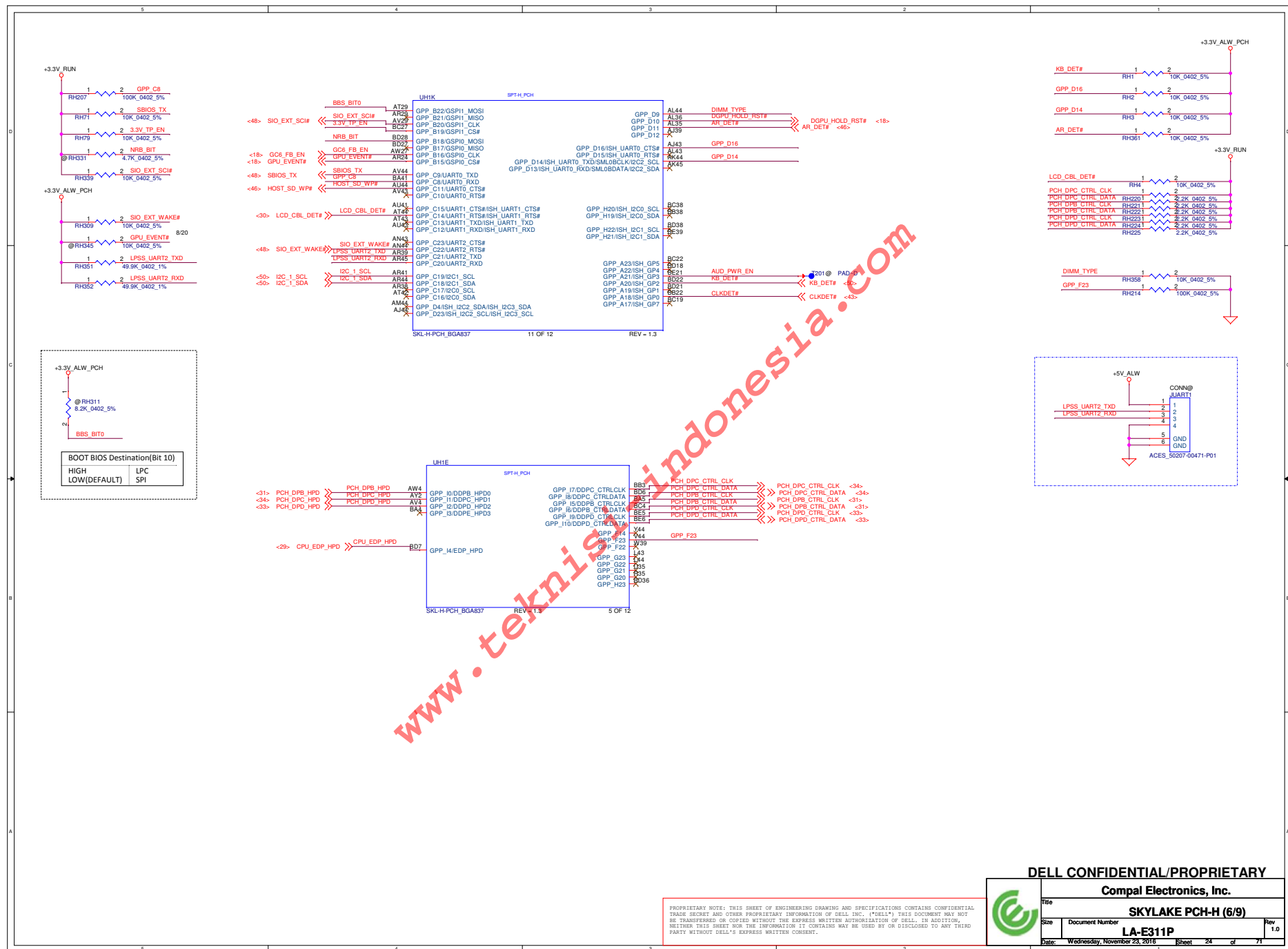


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Title			
SKYLAKE PCH-H (3/9)			
Size	Document Number	Rev	
	LA-E311P	1.0	
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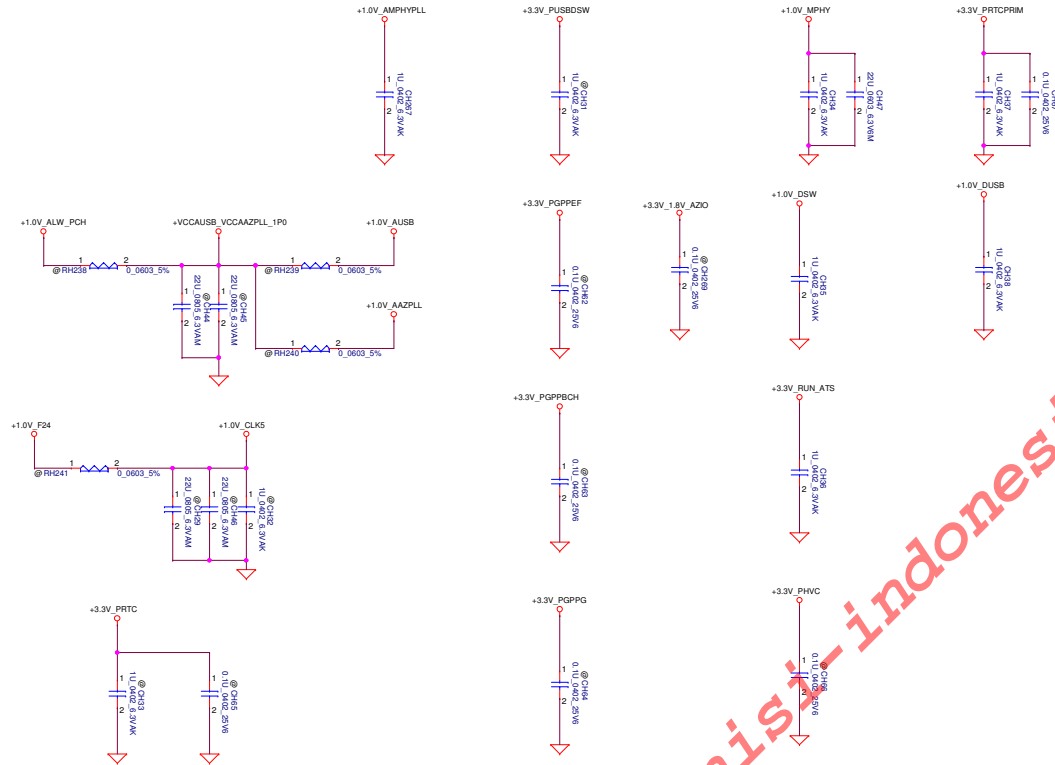
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	Date: <b>Wednesday, November 23, 2016</b> Sheet <b>23</b> of <b>71</b>		







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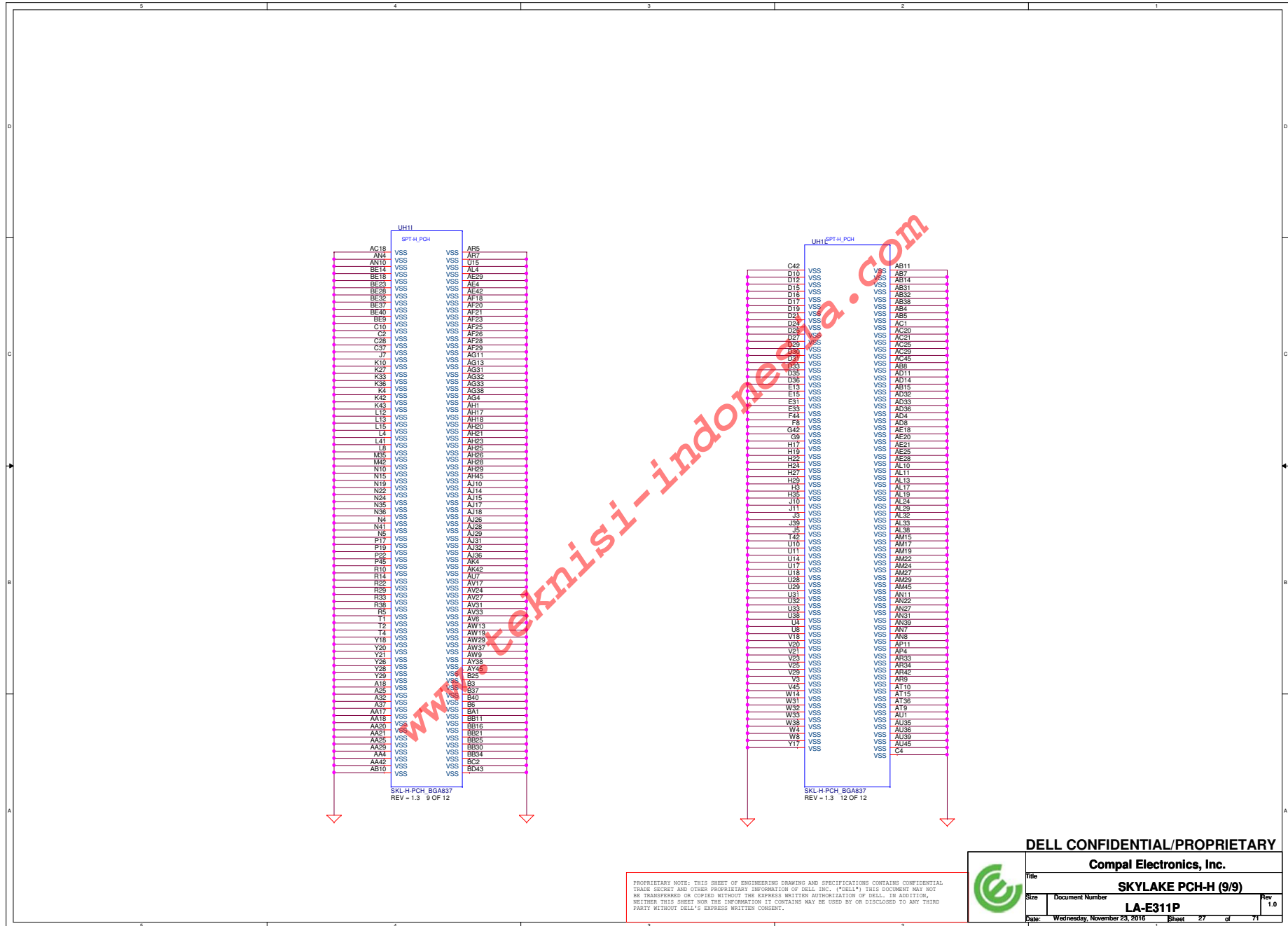
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Size	Document Number	Rev	1.0
LA-E311P			
Date	Wednesday, November 23, 2016	Sheet	27 of 71

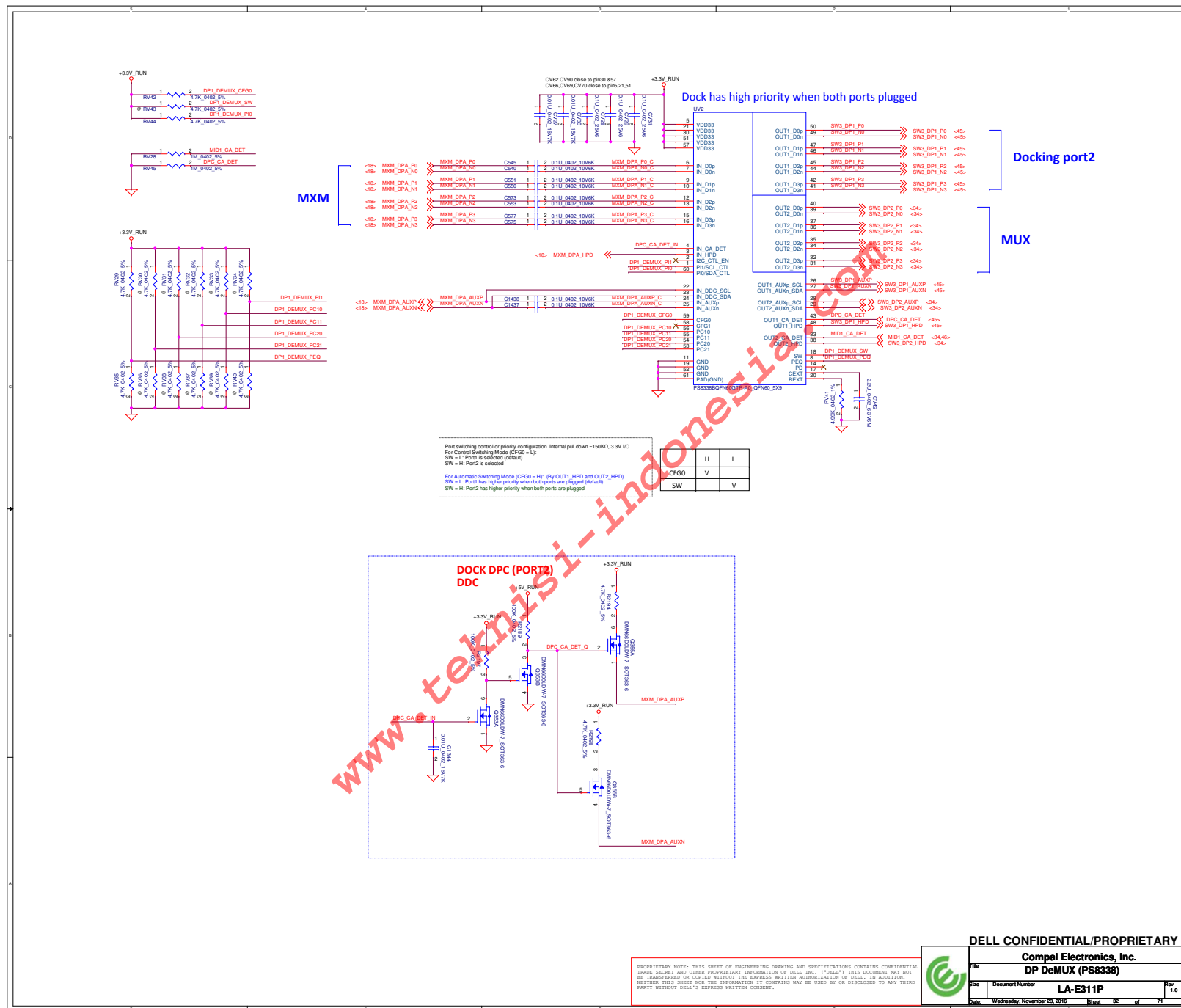
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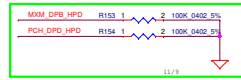






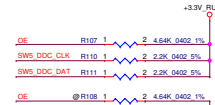
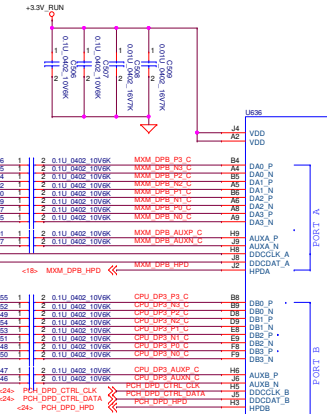
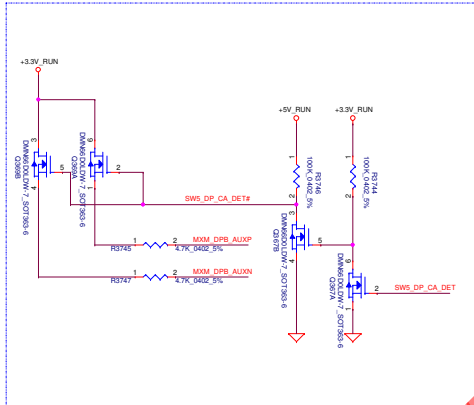






MXM

CPU



OE	Output enable
H	Normal Operation
L (Default)	Standby Mode

DP2\_GPU\_SEL#;

0: 300X	1: i-GPU
DX_SEL	Input
H	Port B
L (Default)	Port A

SWS\_DP\_CA\_DET;

0: DP2	1: HDWM
AUX_SEL	To/From
H	DDC
L (Default)	AUX

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Compal Electronics, Inc.

Rev	Document Number	Rev
1.0	P33-mDP MB DP1.3 MUX (HD3SS214)	1.0
1.0	LA-E311P	1.0
Date	Wednesday, November 25, 2015	Print

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MUX

CPU

TBT/HDMI

DP1\_GPU\_SEL#: 0: MUX; 1: GPU

SW	Input
H	IN2
L (Default)	IN1

PN change to SA00060U10

INy\_PEQ = Programmable input equalization levels  
L: default, LFEQ, compensate channel loss up to 11.5dB @ HBR2  
H: HEQ, compensate channel loss up to 14.5dB @ HBR2  
M: LLEQ, compensate channel loss up to 9.5dB @ HBR2

INy\_AEQ# = Automatic EQ disable  
L: Automatic EQ enable (default)  
H: Automatic EQ disable

PI0 = Auto test enable  
L: Auto test disable & input offset cancellation enable (default)  
H: Auto test enable & input offset cancellation enable  
M: Auto test disable & input offset cancellation disable

PC0 = AUX interception disable  
L: AUX interception enable, driver configuration is set by link training (default)  
H: AUX interception disable, driver output with fixed 800mV and 0dB  
M: AUX interception disable, driver output with fixed 400mV and 0dB

PC1 = Output swing adjustment  
L: default  
H: +20%  
M: -15.7%

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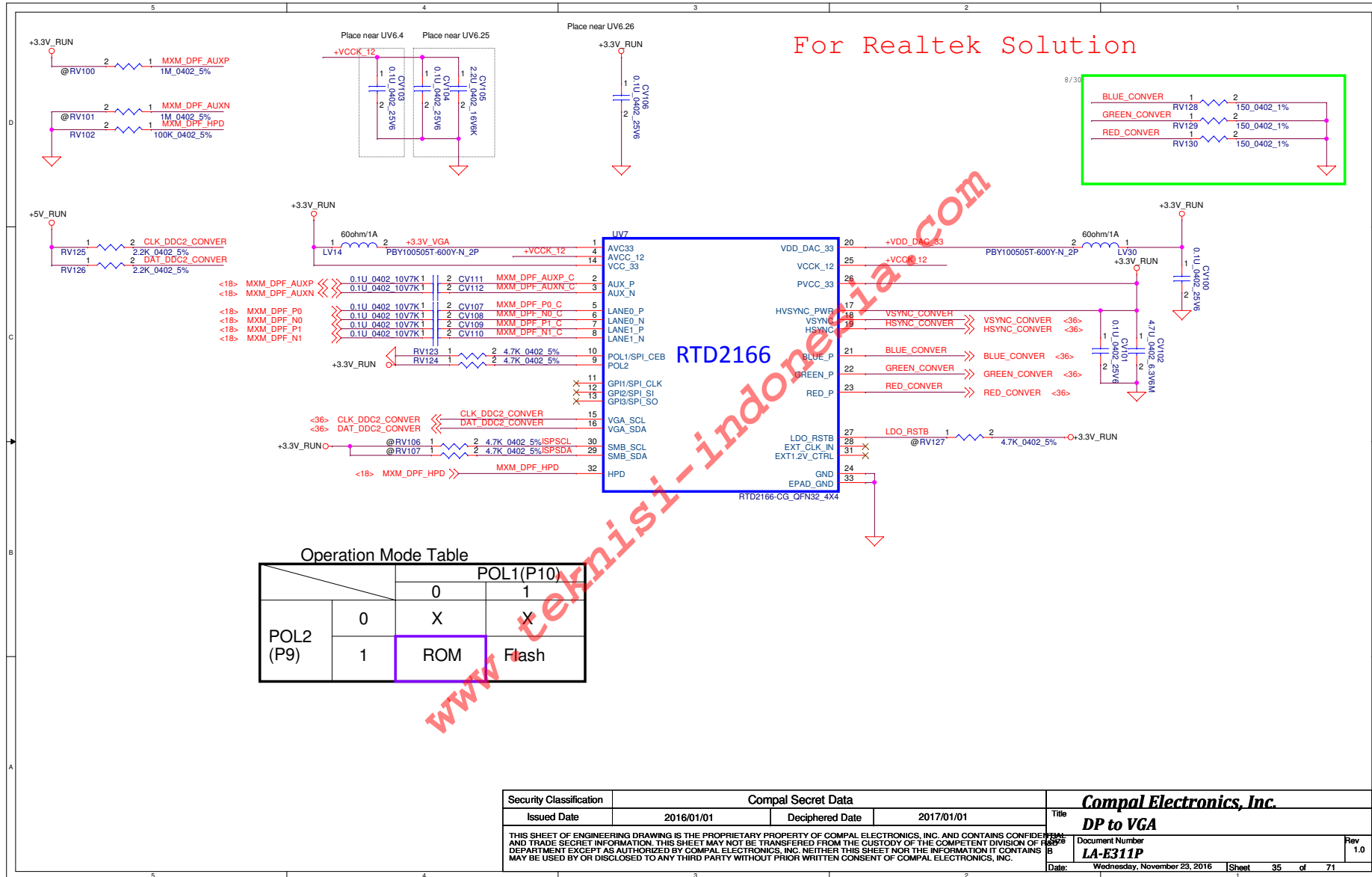
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Rev	VGA CONN		Rev
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For Realtek Solution



From MXM  
From convertor

<18> RED MXM  
<18> GREEN MXM  
<18> BLUE MXM  
<18> HSYNC MXM  
<18> VSYNC MXM  
<18> DAT\_DDC2\_MXM  
<18> CLK\_DDC2\_MXM  
  
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<35> GREEN CONVER  
<35> BLUE CONVER  
<35> HSYNC CONVER  
<35> VSYNC CONVER  
<35> DAT\_DDC2\_CONVER  
<35> CLK\_DDC2\_CONVER

RED MXM  
GREEN MXM  
BLUE MXM  
HSYNC MXM  
VSYNC MXM  
DAT\_DDC2\_MXM  
CLK\_DDC2\_MXM  
  
RED CONVER  
GREEN CONVER  
BLUE CONVER  
HSYNC CONVER  
VSYNC CONVER  
DAT\_DDC2\_CONVER  
CLK\_DDC2\_CONVER

27 B0  
28 B1  
29 B2  
30 B3  
31 B4  
32 B5  
33 B6  
34 C0  
35 C1  
36 C2  
37 C3  
38 C4  
39 C5  
40 C6

UV16  
SEL1  
SEL2  
GND  
GND  
GND  
GPAD

1 A0  
2 A1  
3 A2  
4 A3  
5 A4  
6 A5  
7 A6  
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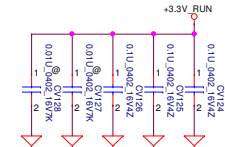
RED DOCK  
GREEN DOCK  
BLUE DOCK  
HSYNC DOCK  
VSYNC DOCK  
DAT\_DDC2 DOCK  
CLK\_DDC2 DOCK  
  
NEW MXM SELECT  
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RED DOCK <45>  
GREEN DOCK <46>  
BLUE DOCK <45>  
HSYNC DOCK <46>  
VSYNC DOCK <45>  
DAT\_DDC2 DOCK <46>  
CLK\_DDC2 DOCK <45>

TS3V712ERTOR\_QFN32\_8X3

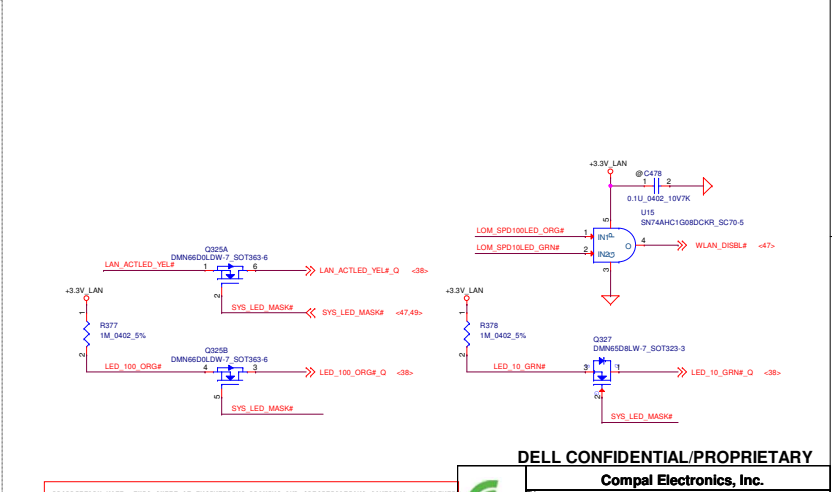
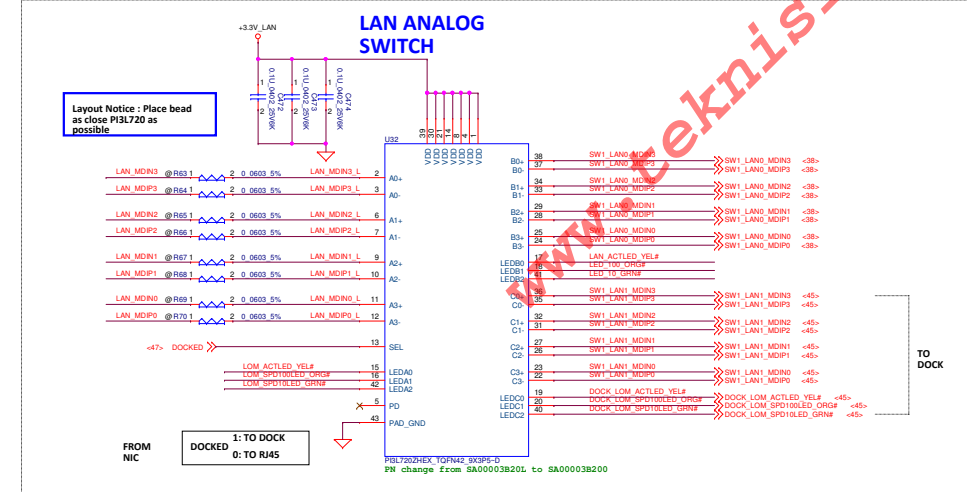
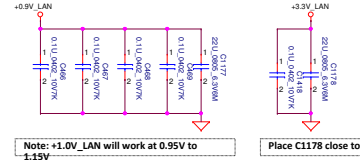
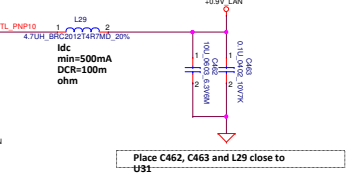
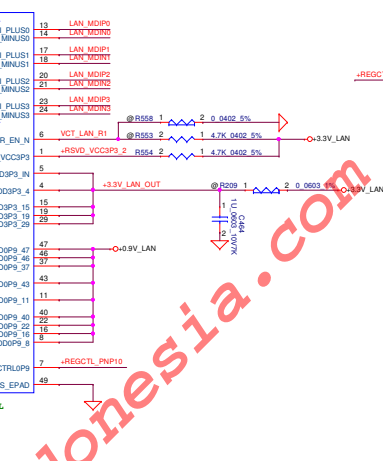
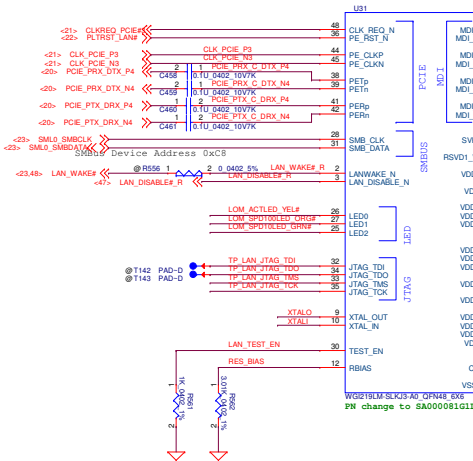
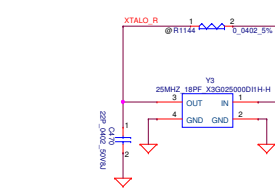
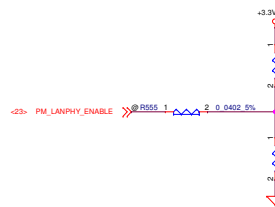
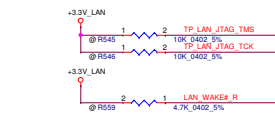
To VGA DOCK

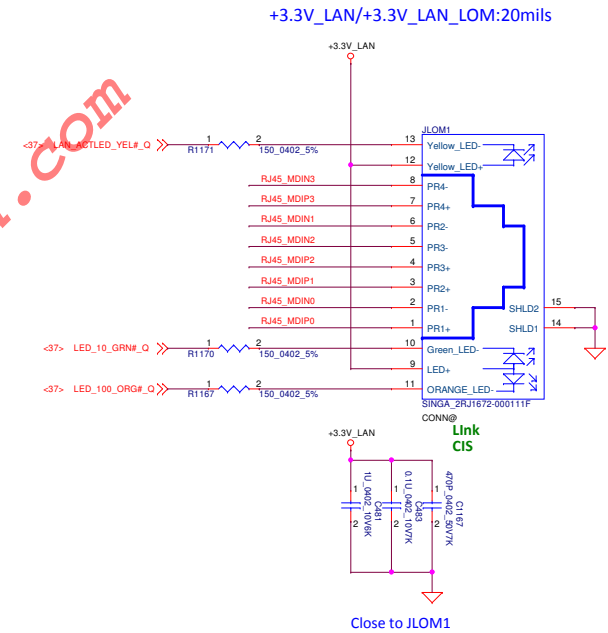
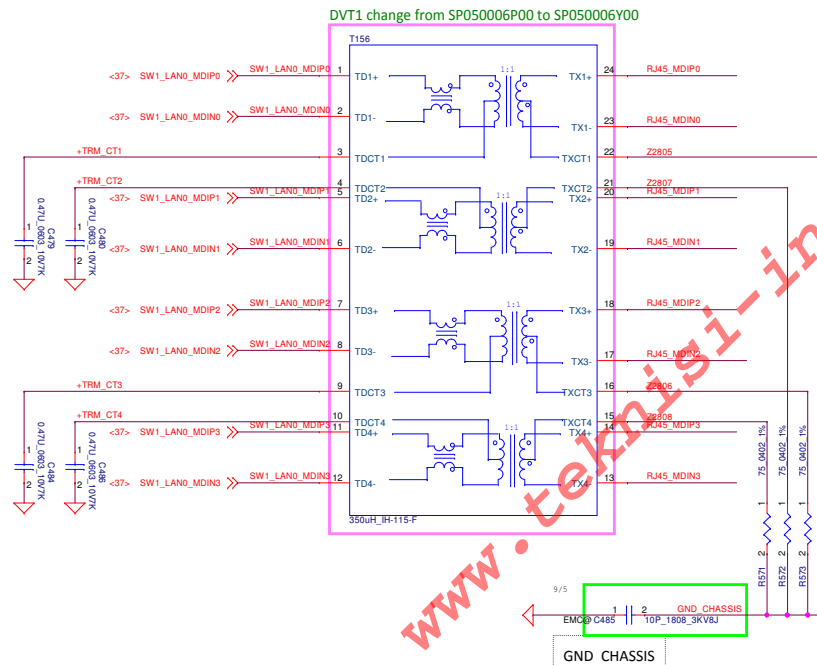
MXM_SELECT	Chanel	Source
0	A=B1	MXM_VGA
1	A=B2	CONVERTER



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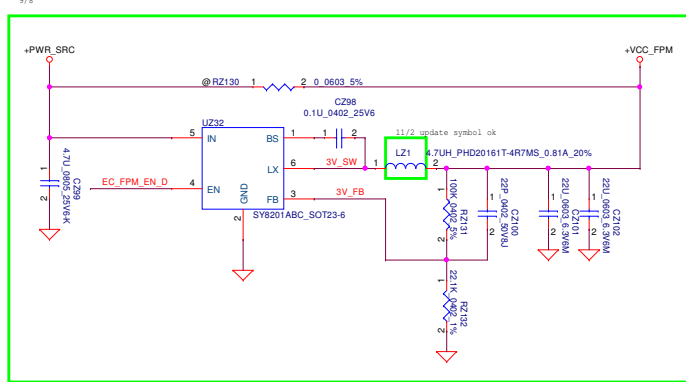
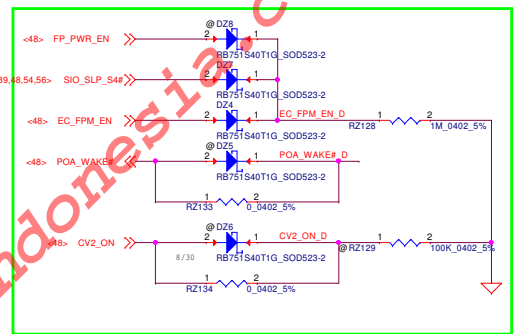
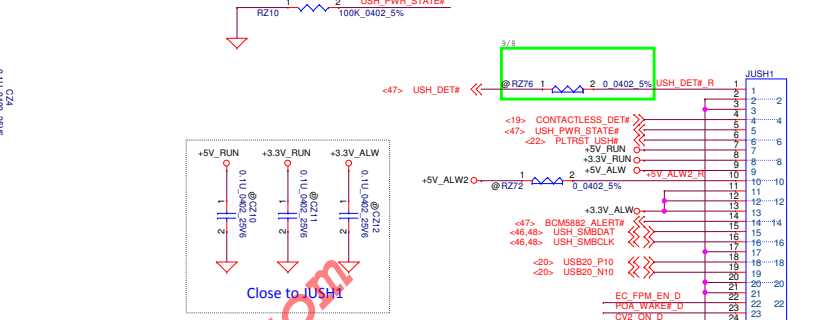
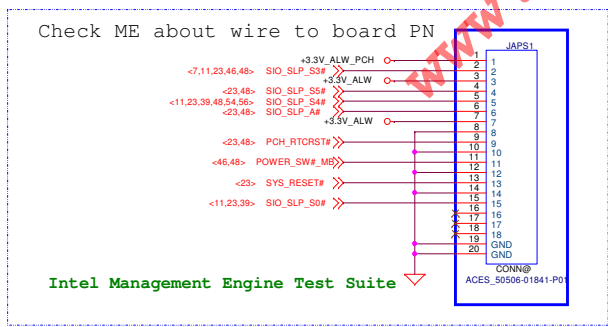
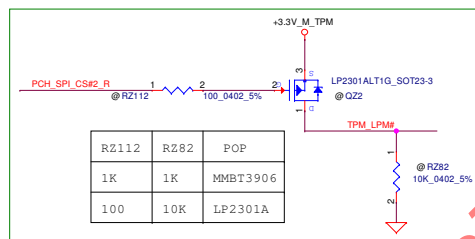
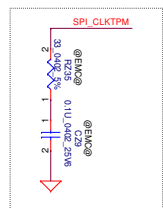
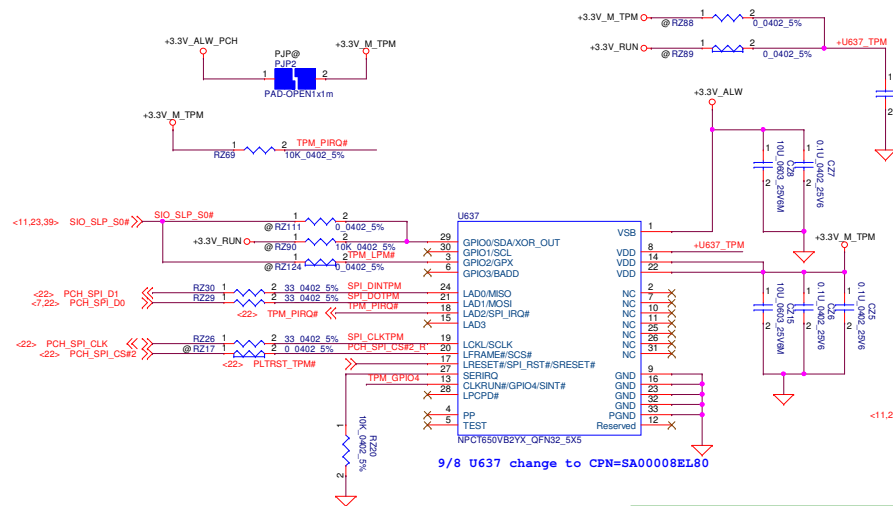
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				Size	Document Number
				Customer	L4-E311P
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RJ45			
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TPM/USH

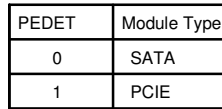
LA-E311P

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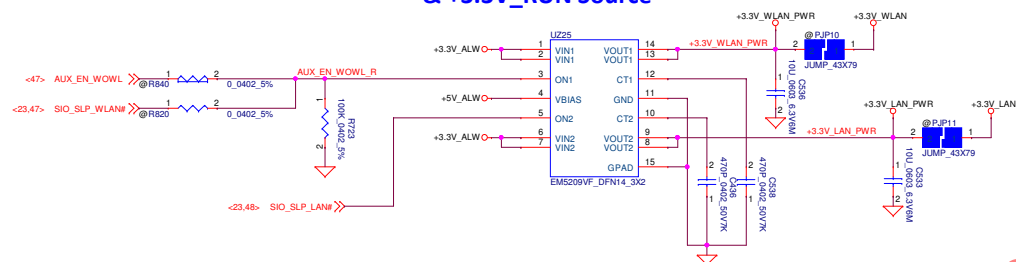
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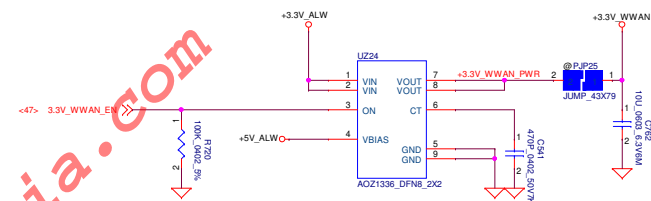


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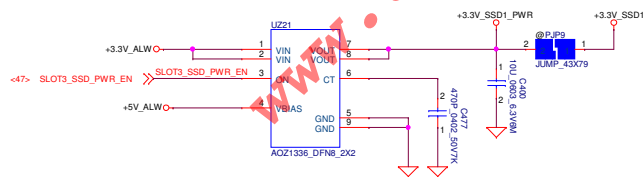
### Power Control for M.2 slot 1. & +3.3V\_RUN Source



### Power Control for M.2 slot 2.



### Power Control for M.2 slot 3: Source



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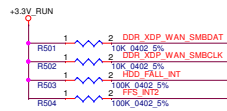
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M.2 Card PWR

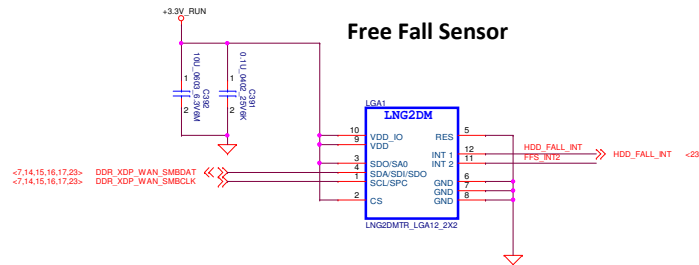
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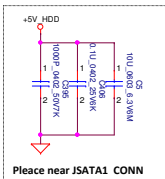
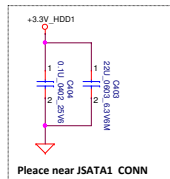
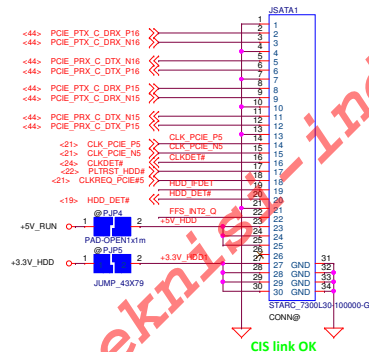
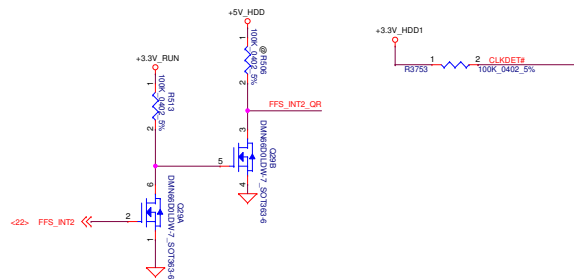
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## Free Fall Sensor



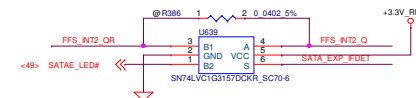
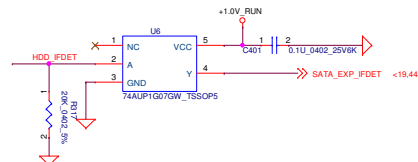
## HDD1 CONN



HDD_IFDET	DEVICE interface
0	SATA
1 (1.44V)	PCIE

SATA_EXP_IFDET	DEVICE interface
0	SATA
1 (3.3V)	PCIE

SATA_EXP_IFDET	channel on
0	A-->B1
1	A-->B2



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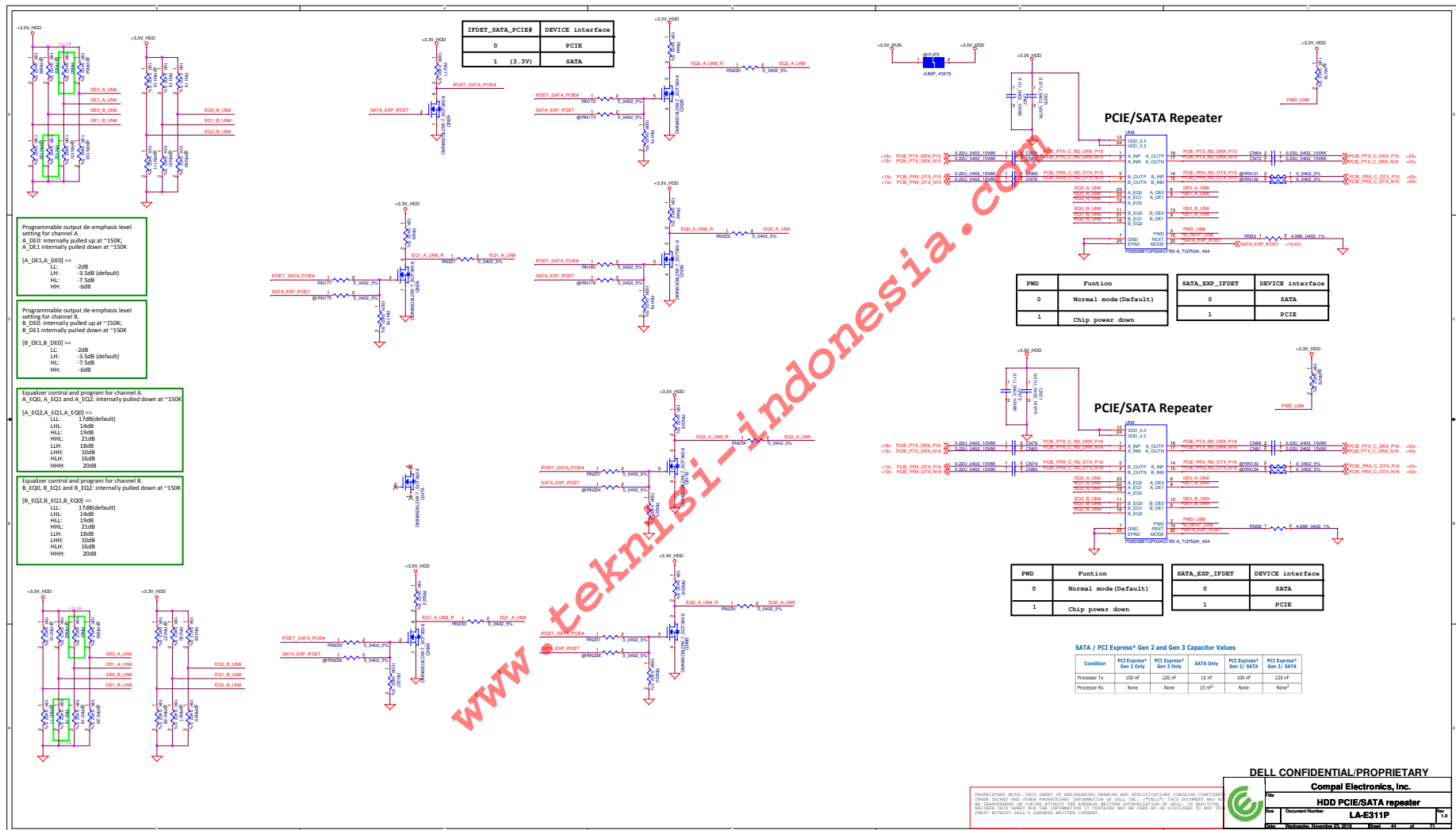
Compal Electronics, Inc.

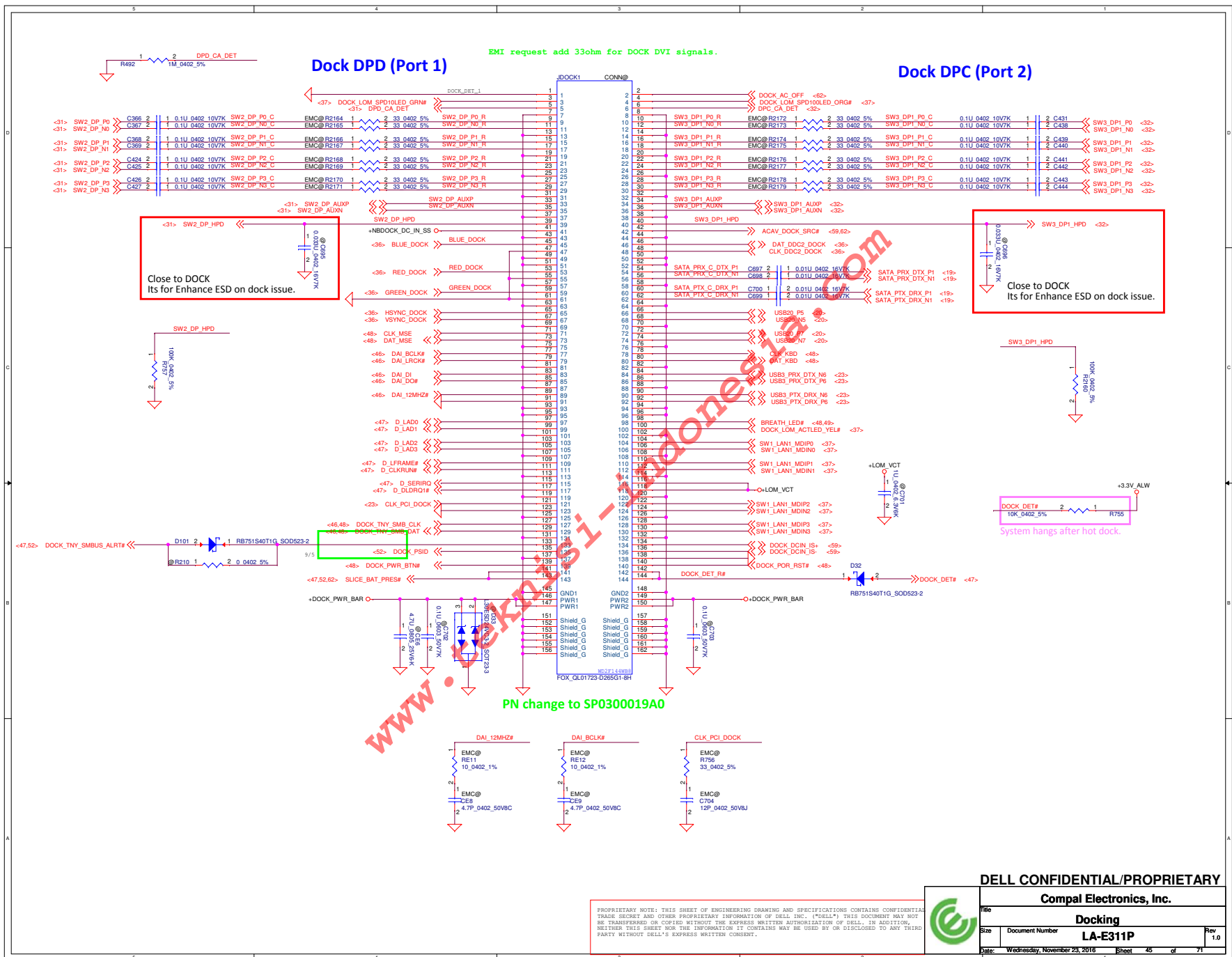
HDD CONN

LA-E311P

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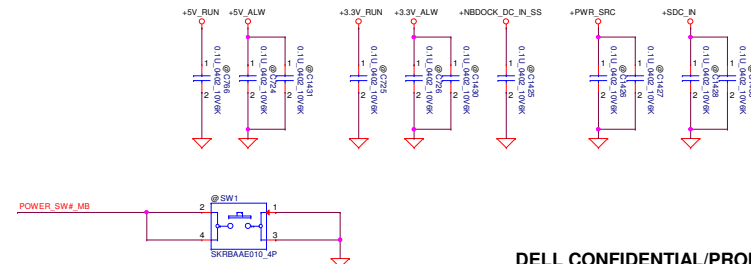
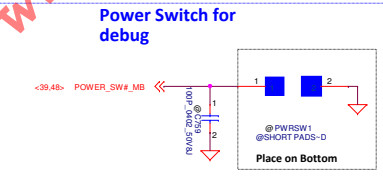
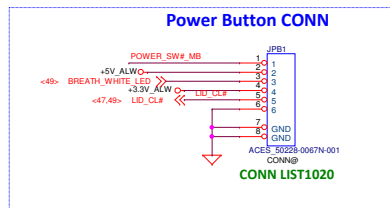
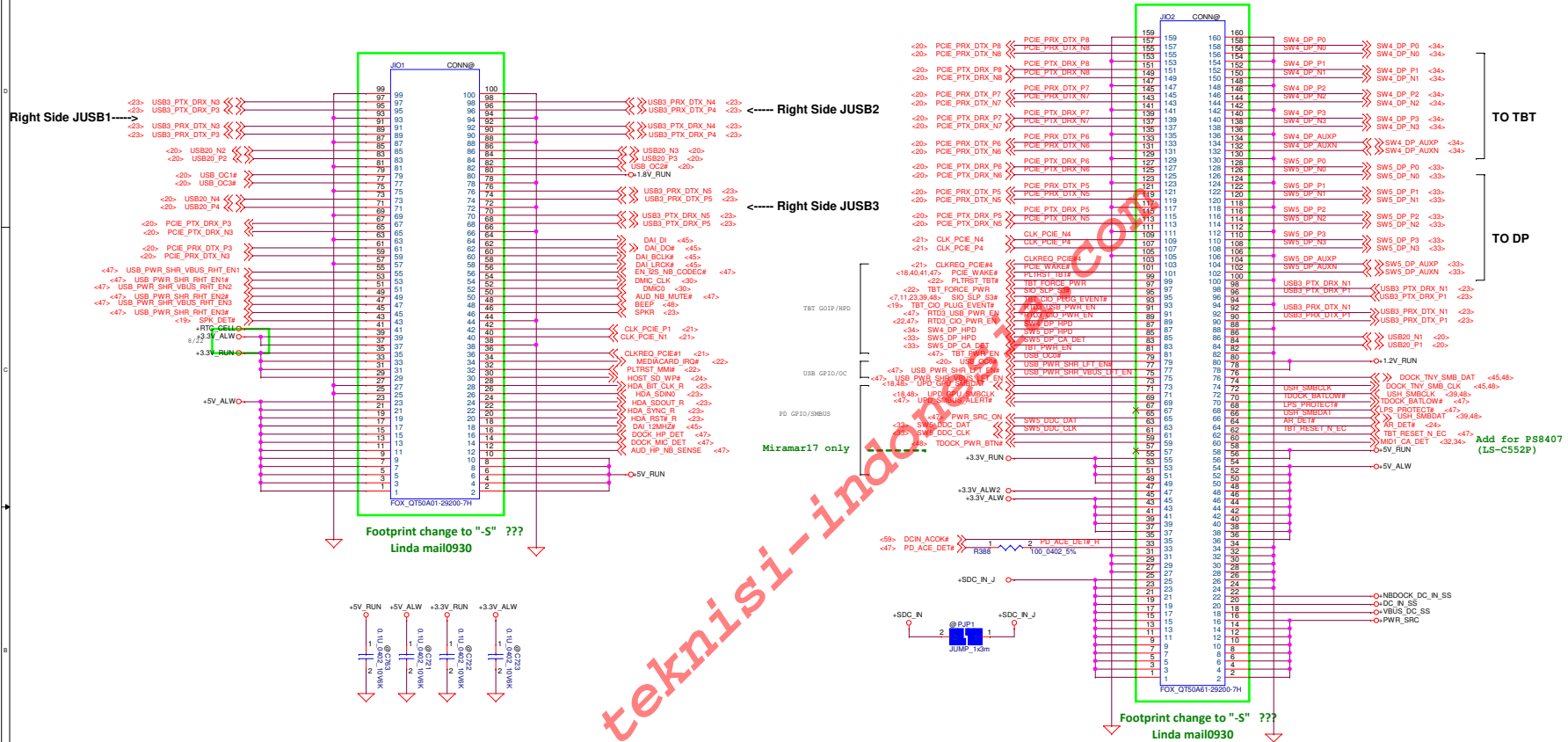
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# USB/Codec/Card reader IO/B

# Display daughter /B



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IO / PWR Button

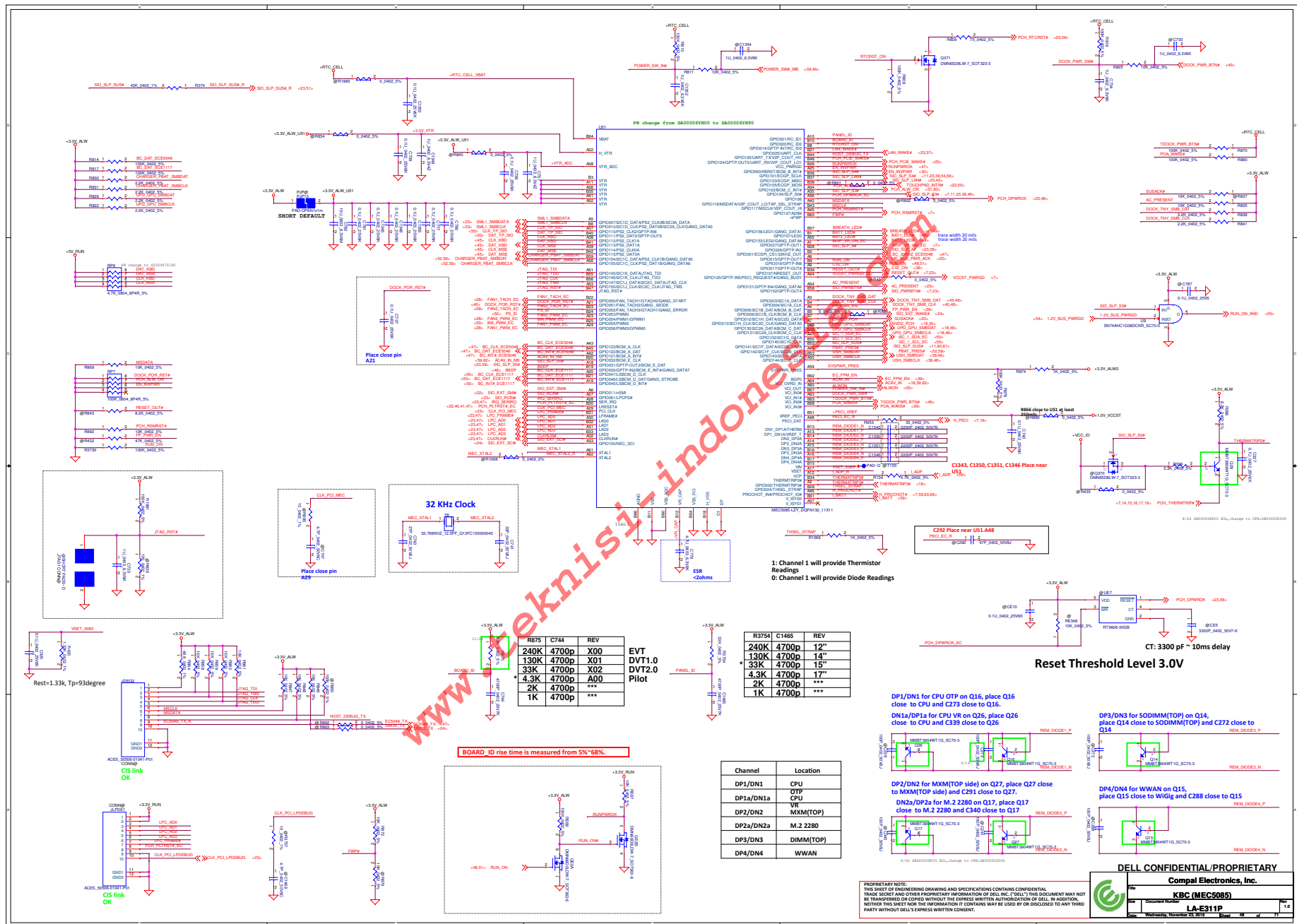
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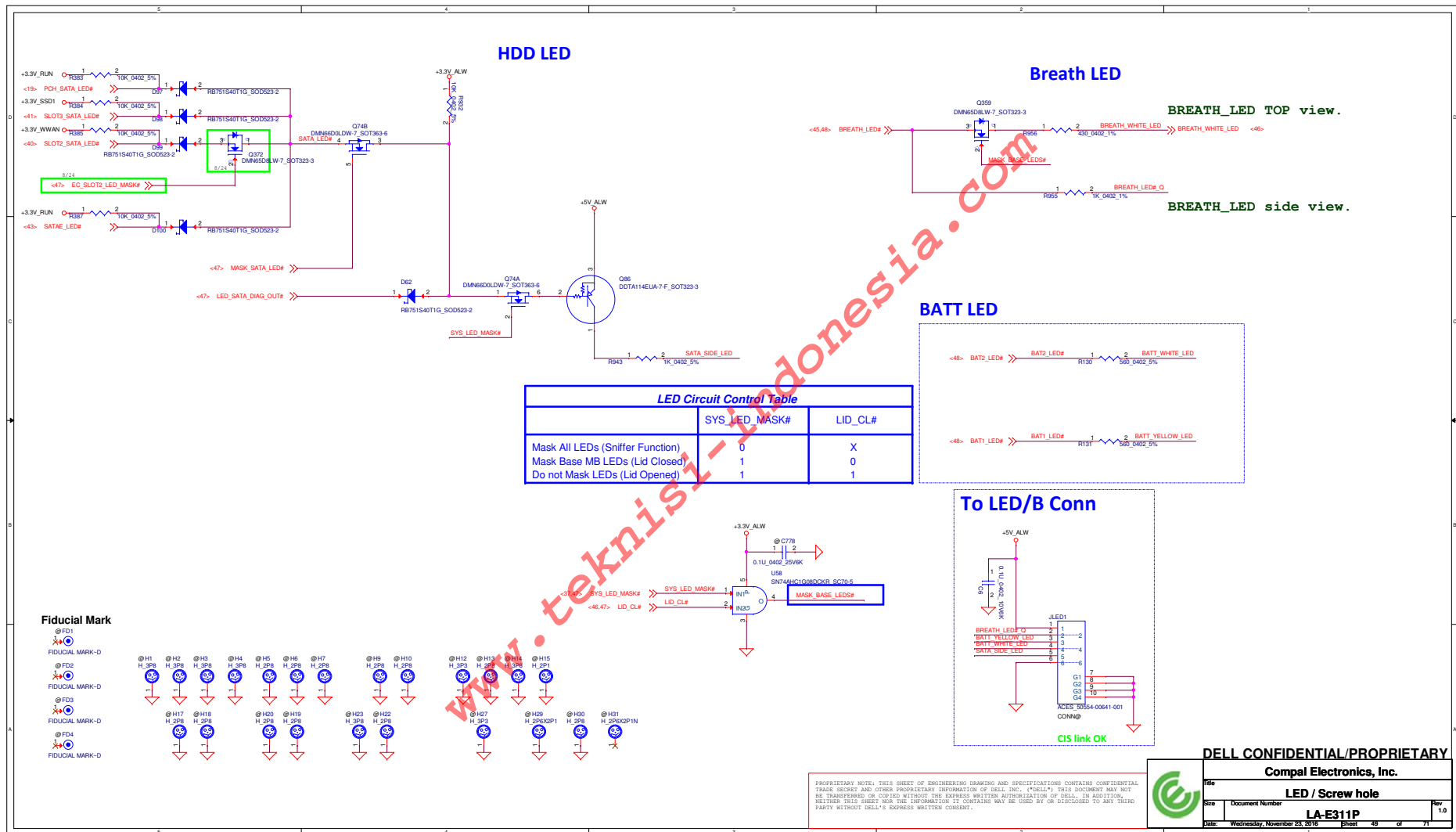
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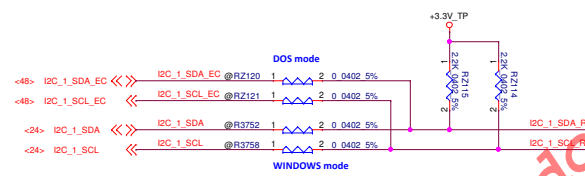
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Size: Document Number  
Date: Wednesday, November 25, 2016  
Sheet: 46 of 71









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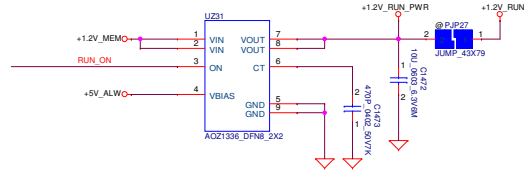
Place close to JKBTP1

The diagram illustrates a circuit for I2C bus termination. A +3.3V TP supply is connected to a network of resistors. The network includes resistors R2114, R2115, and R2116. The I2C\_1\_SDA line is connected to R2114 and R2116, and the I2C\_1\_SCL line is connected to R2115 and R2116. The diagram is labeled 'DOS mode' and 'WINDOWS mode'.

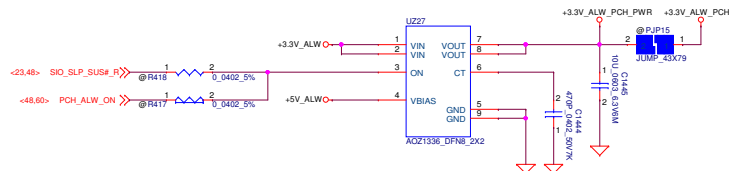
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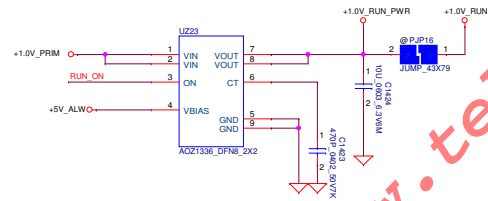
**+1.2V\_RUN Source**



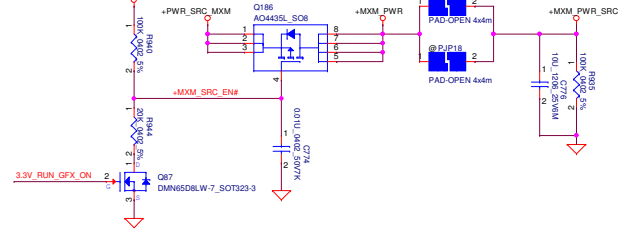
**+3.3V\_ALW\_PCH Source**



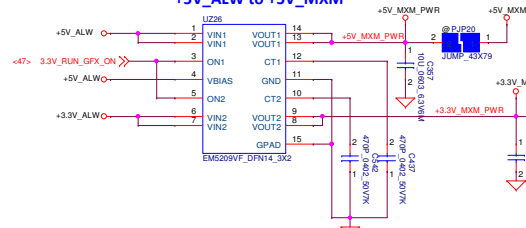
**+1.0V\_PRIM to +1.0V\_RUN**



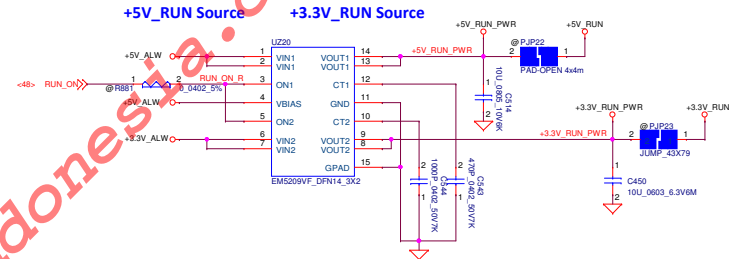
**MXM\_PWR\_SRC Source**



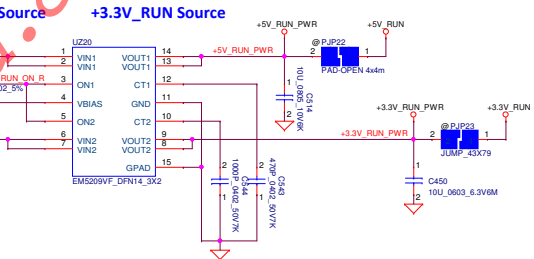
**+3.3V\_ALW to +3.3V\_MXM  
+5V\_ALW to +5V\_MXM**



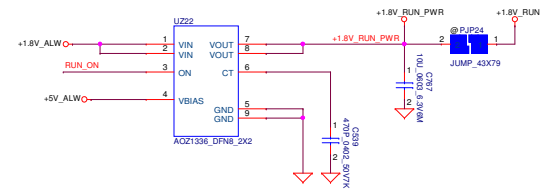
**+5V\_RUN Source**



**+3.3V\_RUN Source**



**+1.8V\_RUN Source**



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Power Control

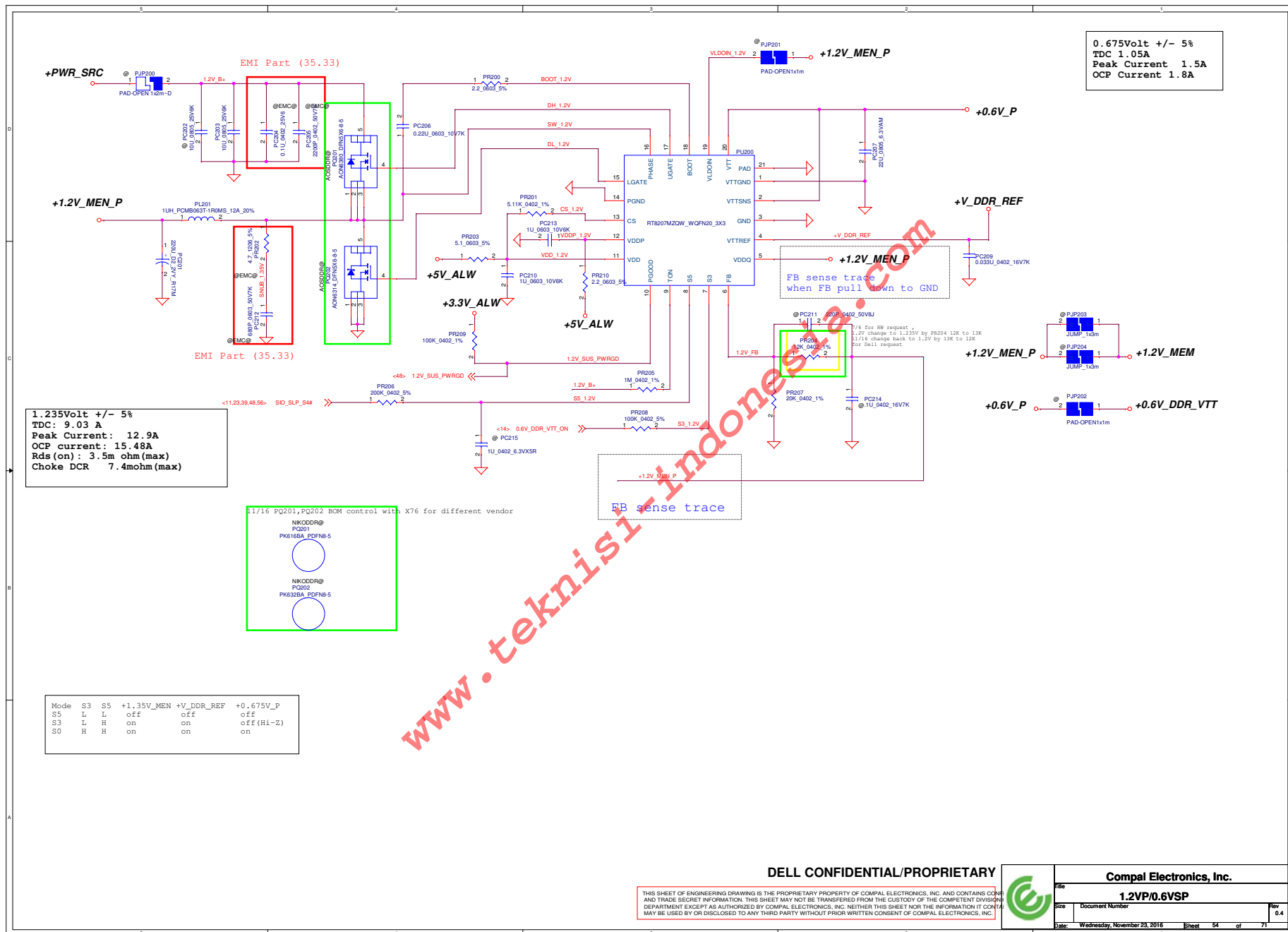
Document Number LA-E311P

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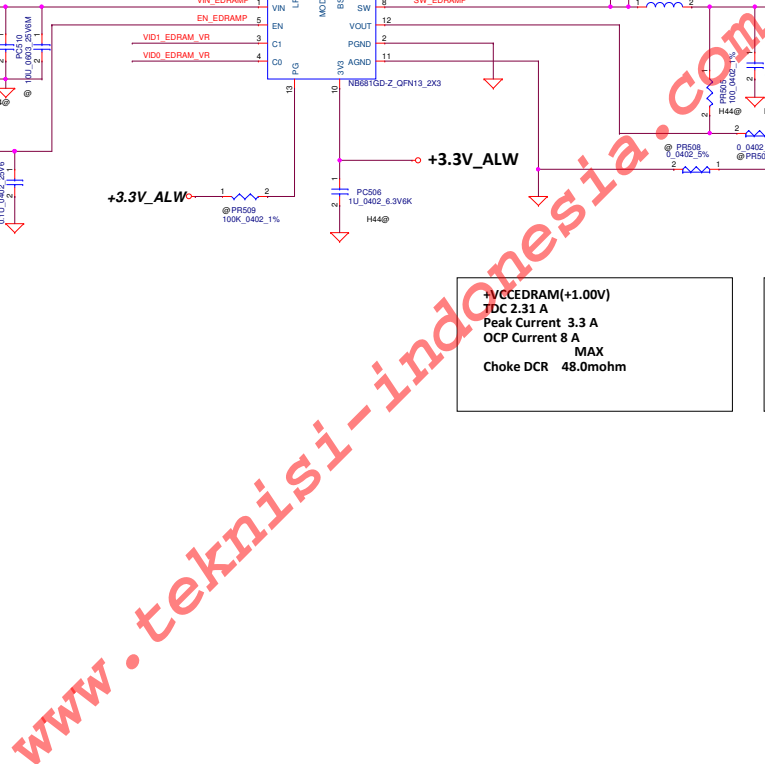








Only H44e



+VCCEDRAM(+1.00V)  
TDC 2.31 A  
Peak Current 3.3 A  
OCP Current 8 A  
MAX  
Choke DCR 48.0mohm

proximal	PR505 0ohm	PR506 100ohm	PR508 100ohm
remote	PR505 100ohm	PR506 0ohm	PR508 0ohm

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+VCCEDRAM, 1V

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23, 2016 Sheet

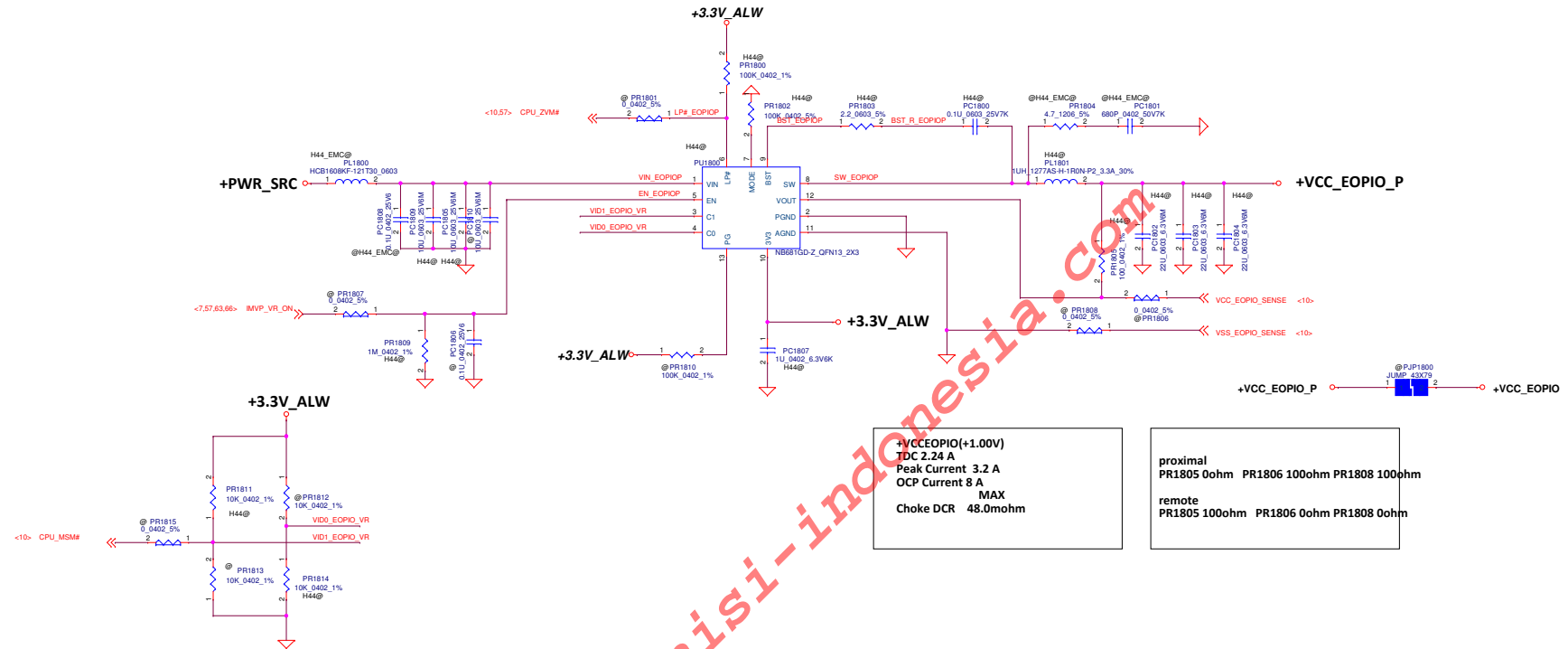
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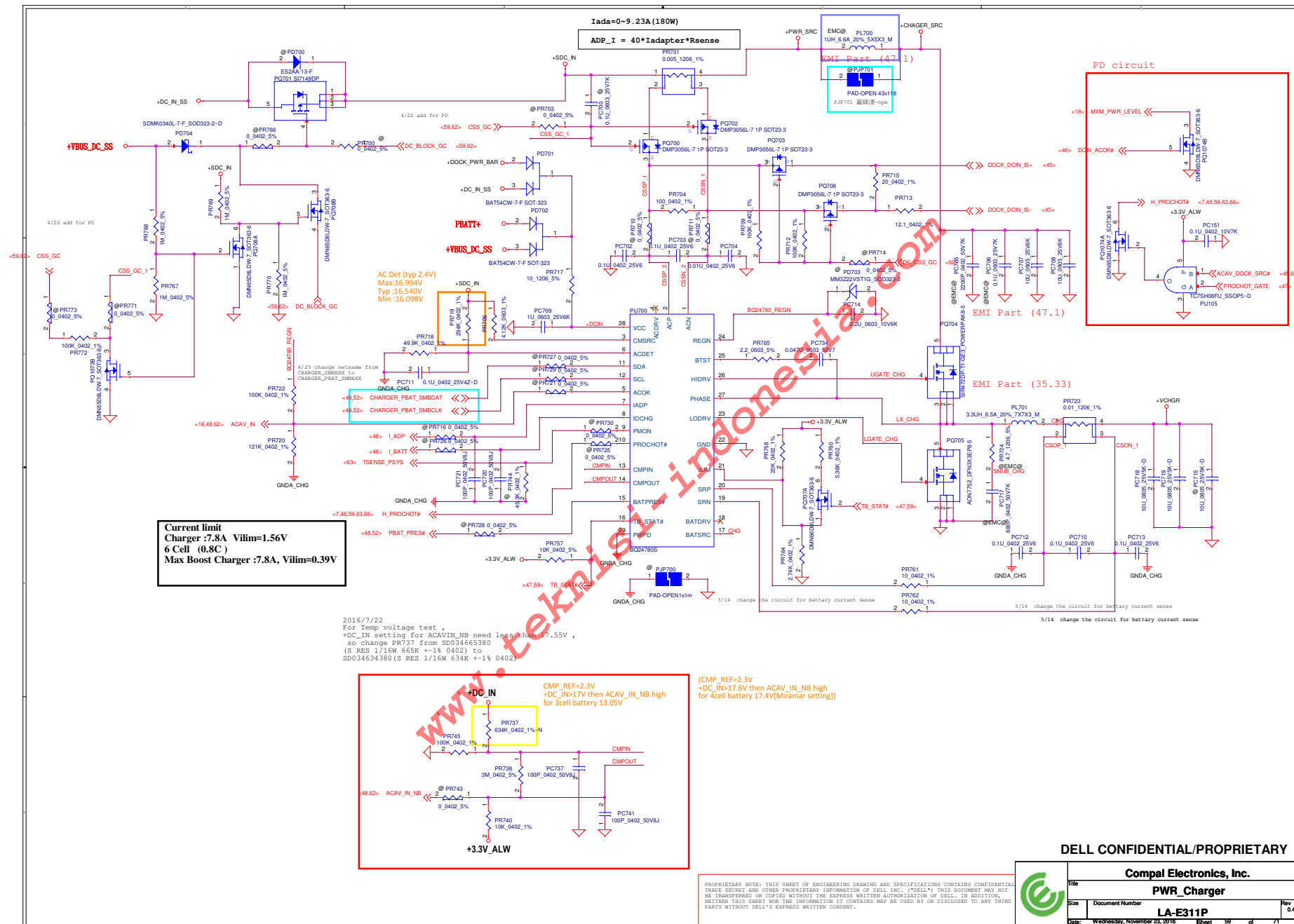
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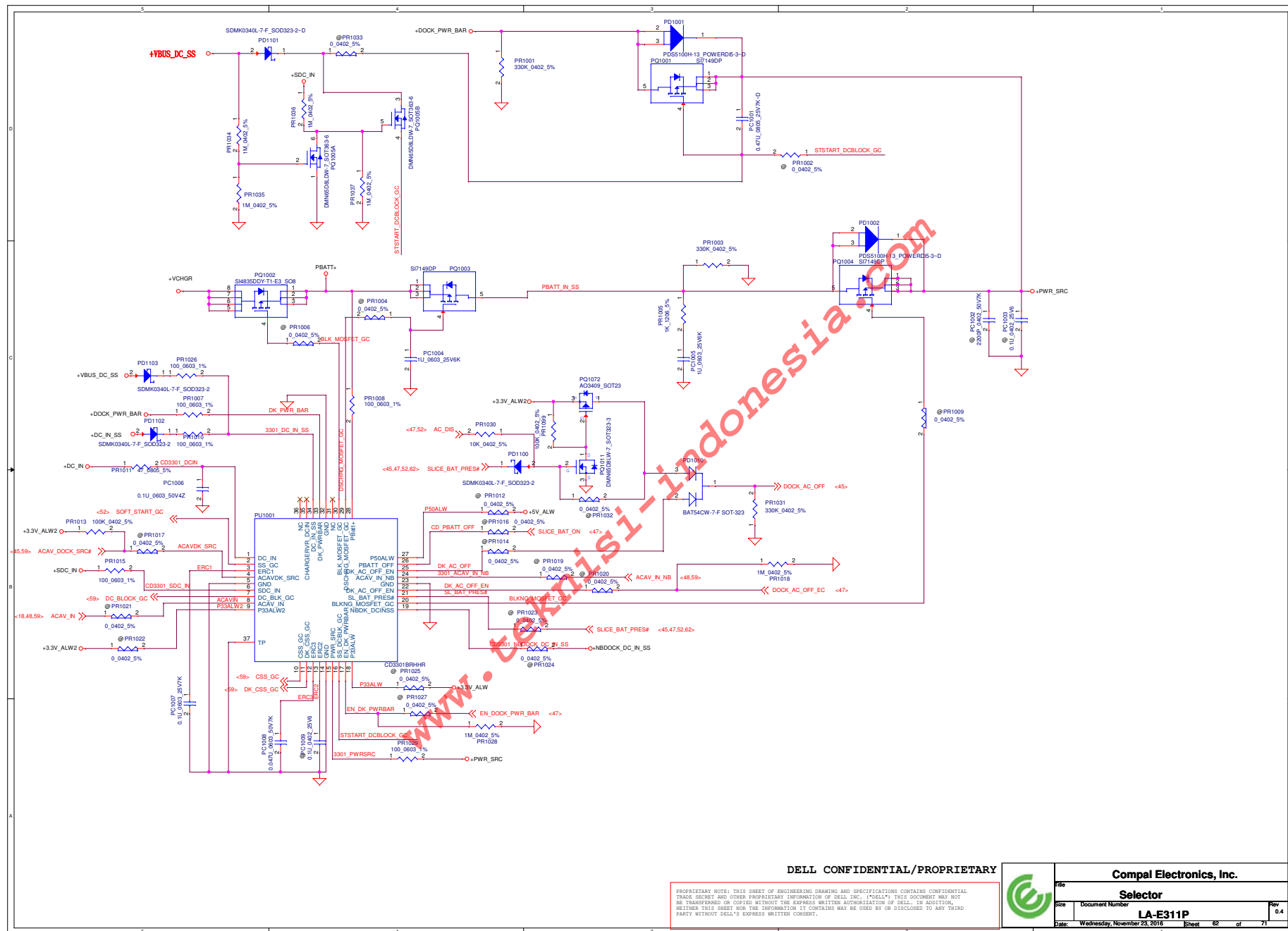
Date Wednesday, November 25, 2015 Sheet 08 of 71

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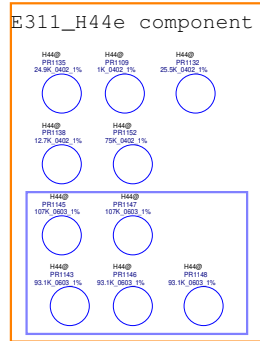


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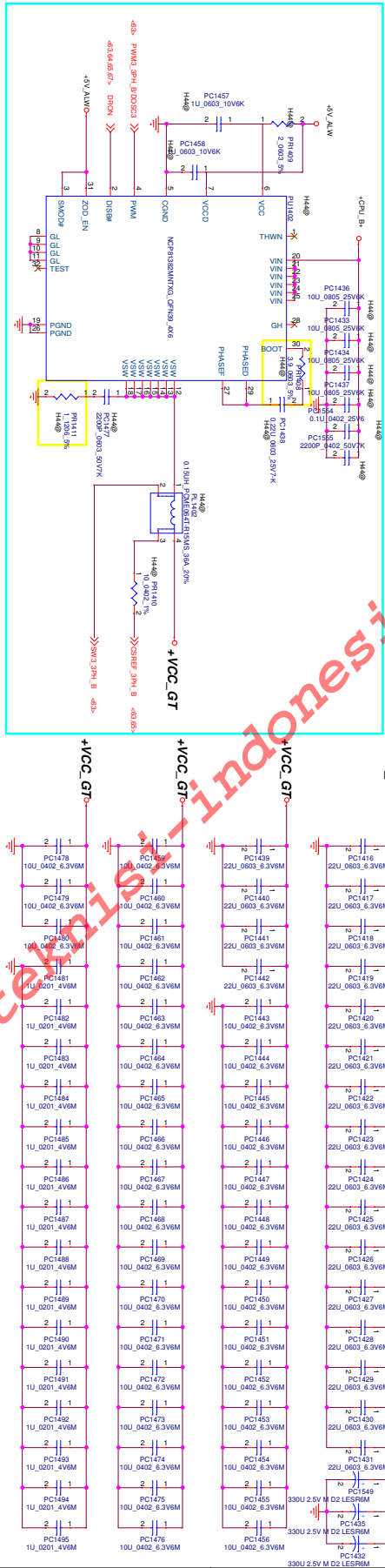
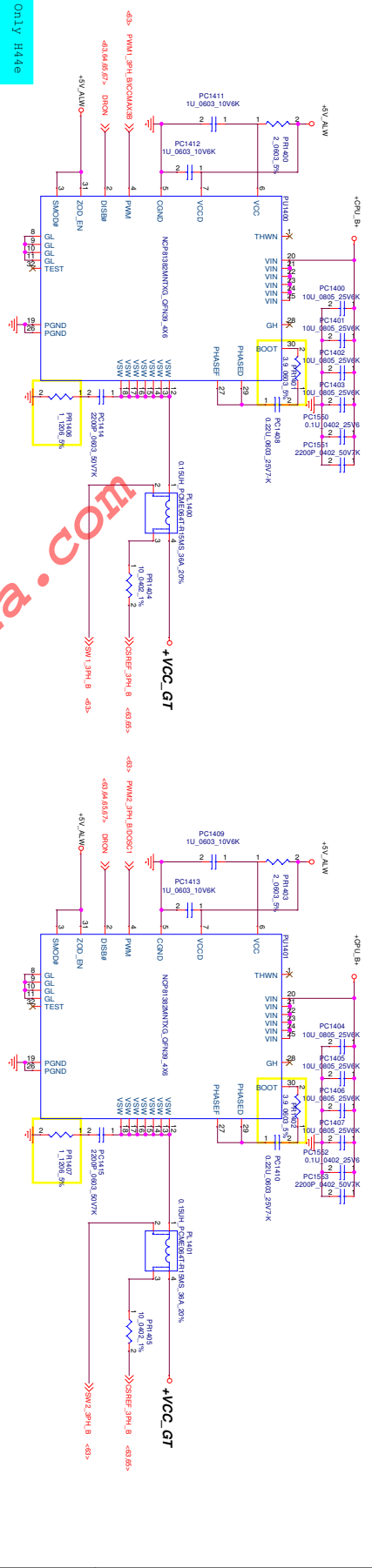


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+VCC_GT:	H44e	H42
TDC:	70A	25A
Peak Current	94A	55A
Choke Idc:	36A / 1sat:	45A
DCR	0.66mohm	+7%

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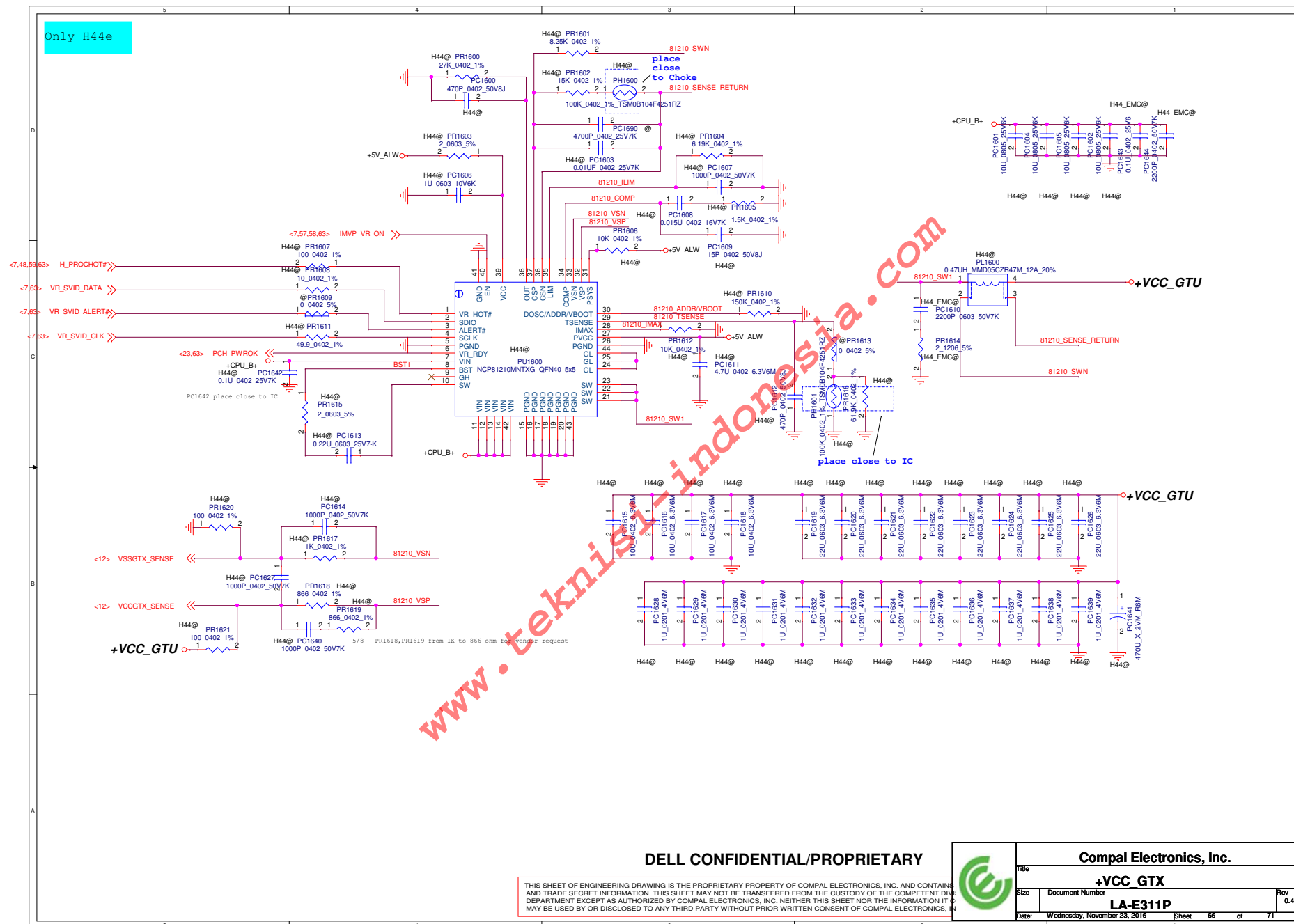
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# Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	29	HW	2016/06/01	compal	system can't dispaly on eDP panel	change CPU_EDP_HPD to U630.3 and MXM_EDP_HPD to U630.13	0.2 (X00)
2	39	HW	2016/06/07	compal	system can't detect USH/B	change R272 to 0ohm short for load sw power to turn on +3.3V_CV2,+3.3V_FPM(EVT pop)	0.3 (X01)
3	33	HW	2016/06/07	compal	mDP can't display	change HD3SS214 operate mode change from stand by mode to normal mode,pop R107,depop R108(EVT pop)	0.3 (X01)
4	39	HW	2016/06/07	compal	Reserve for version B TPM IC design	add BR2124	0.3 (X01)
5	14,17	HW	2016/06/07	compal	change 330uF cap placement for 1pcs/1channel	pop CD25,depop CD43	0.3 (X01)
6	48	HW	2016/06/07	compal	For press power button over 20 sec,EC can sent RTCRST_ON to reset RTC	add R808,R809,Q371,and connect R808.1,Q371.2 to U51.B8	0.3 (X01)
7	38	HW	2016/06/23	compal	change C481 package size from 0603 to 0402	change C481 from SE080105K80 to SE00000Q1L10	0.3 (X01)
8	46	HW	2016/06/28	compal	prevent damage with Miramar I/O board	J101 rotate 180 degree.	0.3 (X01)
9	19	HW	2016/06/28	compal	TBT_CIO_PLUG_EVENT# pull up change from +3.3V_ALW to +3.3V_ALW_PCH for power leakage	TBT_CIO_PLUG_EVENT# add RH366 pull to +3.3V_ALW_PCH, de-pop RH341	0.3 (X01)
10	48	HW	2016/07/01	compal	reserve for DFWROK sequence	add @UE7,@CES,@CE10,@E348,change R802 from 0ohm-short to 0ohm and pop it.	0.3 (X01)
11	48	HW	2016/07/01	compal	Board ID change to X01	change R875 from 240Kohm to 130Kohm	0.3 (X01)
12	39	HW	2016/07/01	compal	TPM leverage X8	change R2111 from 0ohm-short to 0ohm,depop R2111,R2112,R282,Q22,pop R2124	0.3 (X01)
13	39	HW	2016/07/01	compal	USH	change R210 from 4M to 100Kohm,depop D23,pop R276	0.3 (X01)
14	40	RF	2016/07/01	compal	leverage X8-reserved 0 ohm on COEX1-3 between WWAN and WLAN	add R2125,R2126,R2127	0.3 (X01)
15	47	HW	2016/07/04	compal	leverage X8-TBT_RESET_N_EC add R886 PD 100Kohm	add R886	0.3 (X01)
16	25	RF	2016/07/05	compal	5.76G noise mitigation	change RH362,RH363 from 0ohm to bead(BLM15GA750SN1) and location change to LH1,LH2	0.3 (X01)
17	33	HW	2016/07/07	TI	HD3SS214ZQER SPEC pin define error	change SW5_DP_N1 from U636.E2 to U636.E1, SW5_DP_P1 from U636.E1 to U636.E2	0.3 (X01)
18	46	HW	2016/08/22	compal	support RIO USB3.0 wake on WWAN in S3	change J101.37 from +3.3V_RUN to +3.3V_ALW	0.4 (X02)
19	48	HW	2016/08/22	compal	Board ID change to X02	change R875 from 130Kohm to 33Kohm	0.4 (X02)
20	7	HW	2016/08/22	compal	DCI enable on KBL-H	change RC314,RC315 BS from @XDP@ to XDP@	0.4 (X02)
21	7	HW	2016/08/24	compal	leverage X8-aviod system always re-boot	change RC316 to 3Kohm and BS from XDP@ to always pop	0.4 (X02)
22	47,49	HW	2016/08/24	compal	BITS293066: HDD LED keeps lighting when WWAN Card installed	add Q372 and Q372.2 connect to U46.B1(EC_S10T2_LED_MASK#),remove T165	0.4 (X02)
23	18,21	HW	2016/08/25	compal	add CLK_REQ# isolation for N17P/N17E MXM card	change QH3 to Q6 and connect Q6.1 to CLKREQ_PEG#0,Q6.2 to DGPU_FWROK,Q6.3 to MXM_CLK_REQ#,depop R1978	0.4 (X02)
24	48	HW	2016/08/26	compal	SB000008P00 EOL	change Q14,Q15,Q16,Q17,Q26,Q27,Q28 to SB00000Z500	0.4 (X02)
25	18,47	HW	2016/08/29	compal	support UMA detect for VGA ID	add @R1973 between UH1.T45 and U46.B59,depop R803,pop R800	0.4 (X02)
26	39	HW	2016/08/29	compal	add USH protect circuit for EC	add D24,R025,R026,D27,D28,R2128,R2129,U232,R2130,R2131,R2134,CE98-CE102,L21,remove @R270,@R273,change JUSH1.25 to NC,JUSH1.26 to +VCC_FPM,depop R432	0.4 (X02)
27	18	HW	2016/08/30	Nvidia	vender suggest	pop R3750 as default for DGPU_PEX_RST# to avoid EC/PCH electrical timming error	0.4 (X02)
28	35	HW	2016/08/30	compal	CRT impedance match to 75ohm on RV6,B	add PD 150ohm (RV128,RV129,RV130) on RED_CONVER, GREEN_CONVER, BLUE_CONVER	0.4 (X02)
29	39	HW	2016/08/30	compal	Fix 5085 BGP0 behavior abnormal when surprise power shut down with POA disable	add D27 between natname RUN_ON and EC_FPM_EN_D	0.4 (X02)
30	45	HW	2016/09/01	compal	add Docking protect circuit for EC	add D101,@R210	0.4 (X02)
31	38	HW	2016/09/05	compal	EMI EA	change C485 from 150pF to 10pF	0.4 (X02)
32	11,12	HW	2016/09/08	compal	reduce ripple of +1.0V_VCCST,+1.0V_VCCSTG, +1.0V_PRIMP	change C282, C288, CC195,CC186,C263,CZ90 to 10uF_0402	0.4 (X02)
33	39	HW	2016/09/08	compal	leverage X8-change TPM MPN to NPCT650VB2YX	change U637 from SA00008EL70 to SA00008EL80	0.4 (X02)
34	39	HW	2016/09/08	compal	remove reserve component on USH	remove D23,change R276 to 0ohm_short	0.4 (X02)
35	50	HW	2016/09/12	compal	leverage X8-change TP I2C PU R	change R2114,R2115 from 4.7Kohm to 2.2Kohm	0.4 (X02)
36	12,19	HW	2016/09/12	INTEL	PDG1.0	change RH73 from 43ohm to 13ohm,CC187,CC188,C189,CC272 from 22uF to 10uF,depop CC272	0.4 (X02)
37	48	HW	2016/09/19	compal	BITS297377 <Crane 15" DVT1> OTP (Q15)can not meet spec 93+/-3c	pop C273	0.4 (X02)
38	37	HW	2016/09/19	compal	LAN chip change to production PN	change U31 from SA000081G1L to SA000081G3L	0.4 (X02)
39	33	HW	2016/11/09	compal	AMD MXM CARD,display icon SHOW 3 Display when plug 1 monitor	Add R153,R154 PD on MXM_DPB_HPD,PCH_DPD_HPD	1.0 (A00)
40	48	HW	2016/11/23	compal	Board ID change to A00	change R875 from 33Kohm to 4.3Kohm	1.0 (A00)
41	46	HW	2016/11/10	compal	advance BTB connector connection	change J101 from QT50A01-29100-7H to QT50A01-29200-7H,J102 from QT50A61-29100-7H to QT50A61-29200-7H	1.0 (A00)
42	18	HW	2016/11/11	compal	reserve for NV request	add @R155 between U17.1 and U17.2,add R156 between U17.1 and ACAV_IN	1.0 (A00)
43	44	HW	2016/11/18	compal	PCIE IEMT EA-channel A/B de-emphasis level= -6dB/-2dB	pop RN50,RN102,RN61,RN119	1.0 (A00)
44	37,20	HW	2016/11/21	compal	change UH1,U31 to MP part number	change UH1 to SA0000ACM2L,U31 to SA000081G1L	1.0 (A00)

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# Version Change List (P. I. R. List)

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	52 57	POWER	4/29	COMPAL	change PBAT_SMBCLK, CHARGER_SMBCLK PBAT_SMBDAT, CHARGER_SMBDAT net name for HW request	PBAT_SMBCLK, CHARGER_SMBCLK change to CHARGER_PBAT_SMBCLK; PBAT_SMBDAT, CHARGER_SMBDAT change to CHARGER_PBAT_SMBDAT	Rev.01
2	52	POWER	5/4	COMPAL	for EMC request , pop and change PC15 from 0.1U to 1000P	change PC15 from 0.1U(SE042104K80) to 1000P(SE074102K80)	Rev.01
3	53 57	POWER	5/4	COMPAL	for EMI request, need to depop PL100 and PL700	co-layout a jump on PL100 and PL700	Rev.01
4	53 56	POWER	5/12	COMPAL	for DDR4 2400 current request, change output choke to support	1.PL101 change from SH00000YV00 (S COIL 2.2UH +-20% 7.8A 7X7X3 MOLDING) to SH000016700(S COIL 1.5UH +-20% 9A 7X7X3 MOLDING) 2.PL400 change from SH00000YG00(S COIL 1UH +-30% 2.8A 4X4X2 FERRITE) to SH00000IW00 (S COIL 1UH +-20% PCMB042T-1R0MS 4.5A)	Rev.01
5	54	POWER	7/1	COMPAL	for RAM issue , HW request to change from 1.2V to 1.235V	change PR204 from 12K(SD034120280) to 13K(SD034130280)	Rev.03
6	64 65 67	POWER	7/1	COMPAL	For FAE check, pop Dr.MOS EMC part and change bootstrap resistor to reduce the ringing of SW node	change PR1201 PR1202 PR1208 PR1401 PR1402 PR1701 from SD013200B80 (S RES 1/10W 2 +-5% 0603) to SD00000YH00 (S RES 1/10W 3.9 +-5% 0603)	Rev.03
7	64 65 67	POWER	7/11	COMPAL	For FAE check, change snubber resistor to reduce the ringing of SW node	change PR1206 PR1207 PR12011 PR1406 PR1407 PR1702 from SD001200B80 (S RES 1/4W 2 +-5% 1206) to SD011100B80 (S RES 1/4W 1 +-5% 1206)	Rev.03
8	59	POWER	7/22	COMPAL	For Temp voltage test , +DC_IN setting for ACAVIN_NB need less than 17.55V , so change PR737 to achieve	change PR737 from SD034665380(S RES 1/16W 665K +-1% 0402) to SD034634380(S RES 1/16W 634K +-1% 0402)	Rev.03
9	53	POWER	9/2	COMPAL	With compal rule , need to use even part to back to back for acoustic noise improvement so add 3.3V/5V input MLCC to achieve	change PC101,PC102 from SE000000K00(S CER CAP 10U 25V K X5R 0805 H1.25) to SE000006R80(S CER CAP 4.7U 25V K X5R 0805 H1.25) and add PC121,PC122 SE000006R80(S CER CAP 4.7U 25V K X5R 0805 H1.25)	Rev.04

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Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
10	63	POWER	9/2	COMPAL	Change SW to controller resistors size from 0402 to 0603 to improve initial voltage for FAE suggest	change PR1143,PR1146,PR1148 from 82.5K 0402 (SD000002780) to 82.5K 0603 (SD014825280) and PR1145,PR1147 from 56.2K 0402 (SD000001580) to 56.2K 0603 (SD014562280)	Rev.04
11	60 63	POWER	9/2	COMPAL	To improve HW side +1.0V_VCCST ,+1.0V_VCCSTG and +1.0V_VCCSFR output ripple , change 1.0V_PRIM choke and VCCST MLCC	Change PL800 from SH000002200 (S COIL 1UH +-20% 6.6A 5X5X3 MOLDING) to SH00000R810 (S COIL 2.2UH +-20% PCMB053T-2R2MS 5.5A) and PC1101 from SE00000G880 (S CER CAP 0.1U 25V K X5R 0402) to SE00000UD00 (S CER CAP 10U 6.3V M X5R 0402)	Rev.04
12	63	POWER	9/12	COMPAL	For SA Loadline and Iout improvement , modify parameter of VR circuit from FAE suggestion	Pop PC1140 and change from 1000P (SE074102K80) to 2200P (SE074222K80); change PR1107 from short pad to 1K (SD028100180); change PR1109 from 1.43K (SD034143180) to 1.58K (SD000000580); change PR1112 from 30K (SD034300280) to 28K (SD034280280)	Rev.04
13	63	POWER	9/14	COMPAL	For IA,GT Loadline and Iout improvement , modify parameter of VR circuit from FAE suggestion	IA part Change PR1143, PR1146, PR1148 from 82.5K (SD014825280) to 82.7K (SD014887280); change PR1132 from 24.3K to 26.7K (SD034267280); GT part Change PR1145, PR1147 from 56.2K (SD014562280) to 61.9K (SD014619280); change PR1135 from 22.6K to 24.9K (SD034249280)	Rev.04
14	53 59 60	POWER	9/20	COMPAL	For Dell request , 3.3V/5V HS and LS MOS should be used with the same vendor	High side MOS Change PQ100,PQ101,PQ800 from SB000001A00 (S TR SIS412DN-T1-GE3 1N POWERPAK1212-8 to SB00000H800 (S TR AON7408L 1N DFN); Low side MOS Change PQ102,PQ103,PQ705 from SB00000N800 (S TR FDMC7692S 1N MLP to SB000001000 (S TR AON7752 1N DFN3X3EP	Rev.04
15	53	POWER	9/26	COMPAL	For HW request , need to increase 5V output voltage from 5V to 5.08V to reduce PD output voltage drop	Change PR101 from SD034150280 (S RES 1/16W 15K +-1% 0402) to SD034154280 (S RES 1/16W 15.4K +-1% 0402)	Rev.04
16	63	POWER	9/26	COMPAL	To meet intel SPEC for GT voltage , need to modify parameter of VR circuit	Change PR1127 from SD034100180 (S RES 1/16W 1K +-1% 0402) to SD034137180 (S RES 1/16W 1.37K +-1% 0402)	Rev.04
17	53	POWER	11/11	COMPAL	For type C test , change FB resistors to rise output voltage from 5V to 5.156V	Change PR101 from SD034158280 (S RES 1/16W 15.8K +-1% 0402) to SD034154280 (S RES 1/16W 15.4K +-1% 0402); change PR104 from SD028102280 (S RES 1/16W 10.2K +-1% 0402) to SD034976180 (S RES 1/16W 9.76K +-1% 0402)	Rev.10
18	54	POWER	11/11	COMPAL	For 1.2V damage issue , upgrade high side MOS to improve	Change PQ201 from SB00000K300 (S TR SIRA472DP-T1-GE3 1N POWERPAK S08) to SB00000WY00 (S TR SIRA14DP-T1-GE3 1N POWERPAK S08)	Rev.10
19	54	POWER	11/16	COMPAL	For 1.2V damage issue , change HS/LS MOS from Vishay to Magnachop and 1.235V change back to 1.2V	Change PQ201 from SB00000WY00 (S TR SIRA14DP-T1-GE3 1N POWERPAK S08) to SB00000LP00 (S TR AON6380 1N DFN5X6-8); change PQ202 from SB00000WX00 (S TR SIRA06DP-T1-GE3 1N POWERPAKS0-8) to SB00000LGR00 (S TR AON6314 1N DFN5X6-8); change PR204 from SD034130280 (S RES 1/16W 13K +-1% 0402) to SD034120280 (S RES 1/16W 12K +-1% 0402)	Rev.10

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